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LOW COST LOWPOWER FPGA BASED 2D TIME TO DIGITAL CONVERTER

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Abstract: Time-to-digital converters (TDCs) are used as fundamental building blocks in a variety of fields like, digital communication, high-energy physics, Time of Flights (TOF)measurements, biomedical imaging and measurement instrumentation systems. Implementing TDCs in field-programmable gate arrays (FPGAs) has attractive benefits of shorter development Cycle and very less development cost than the ASIC approach. It also offers programming flexibility, which is useful to survive with unpredicted problems and changes in the experimental conditions. We present a low power TDC implemented in a low cost Spartan 3E FPGA device. The converter is based on two level interpolation, in the first level, we used Gray code counter as a coarse counter and a matrices of D Flipflops as a fine interpolation stage. The power consumption of our TDC for a bin size of 5 is 40mw at 500MHz clock frequency.

Keywords-FPGA, TDC, TOF, Digital Communication, measurement instrumentation systems.

I.INTRODUCTION

The TDC has been widely used in many applications such as particle detection in high energy physics, laser range finding, frequency counters, TOF measurements [1] and in positron emission tomography. The performance of a TDC is determined by the resolution, precision, dynamic range, nonlinearity, speed and power consumption. The TDC has been used to measure the time intervals between two rising edges or two electrical timing signals, also called as start and stop signals, which is then quantized and converted into digital data. The delay between the rising edges of the start and stop signals is termed as time delay. The time delay is fed as input to the TDC block shown in figure 1 and the time delay is digitized. The traditional approach in TDC is delay line architecture with delay elements by counting the number of sequential delays that occur within the testing period.

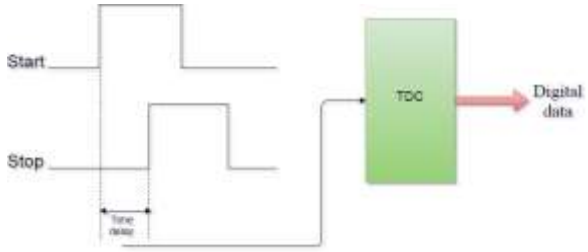

Figure. 1 : Basic TDC block with time delay(delay between the start and stop signals) as input and digital data as output.

Several TDC architectures were proposed - Multichannel tapped delay line based TDC [2], Buffer delay line and RC delay line [3] , Ring oscillator based vernier TDC[4] , Cyclic TDC [5], Tapped Delay Line TDC[6], vernier TDC[7]. Many modifications are made in TDC design to improve parameters like resolution, calibrations(non-linearity, bin-width), dynamic

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range and power consumptions. Some of the works that has been proposed are – (i)The two-level interpolation based on an asynchronous buffer delay line, new RC delay line and LUT-based calibration scheme was developed by Huihua Huang[2] to correct non-linearities , (ii) a TDC prototype with sandwich structure containing 320 time measurement channels (ten TDC daughter cards) was proposed by Jiajun Zheng et.al[8] which is used as digitizer for evaluating super module detectors in compressed baryonic matter(CBM) time-of-fight experiment, (iii) Haochang Chen et.al[6] combined the tuned TDLs and a modified direct-histogram architecture to correct the non-uniformity originated from carry chains, and this TDC does not generate missing codes, (iv) to eliminate the bubble errors in TDC architecture, Yonggang Wang et.al[9] used ones- counter encoder(thermometer-to-binary), (v) Ke Cui et.al[3] proposed an efficient fine time interpolator with period difference recording, which only needs at most thirty one adjustment trials to obtain the required resolution,(vi) Yonggang Wang et.al[1] proposed a new TDL architecture by combining many delay chains to obtain very fine intrinsic cell delays, thus small delay cells in TDL is gained, (vii) Yuan-Ho Chen [7] designed a TDC with dual delay lines which enables real-time calibrations and measures the statistical distribution of delays to allow the calibration of non-uniform delay cells. This DDL-TDC uses FSMs to calibrate the delay in each TDC delay cell thus minimizing DNL values. In this design a coarse counter is added to increase the conversion range, (viii) To reduce the memory requirements the authors, H. Seo and J. Choi[1] proposed mixed-signal TDC with an integrated histogram generation unit (HGU), they were implemented in miniaturised depth-sensor systemson-a-chip (SoCs) for applications in robots, drones and automotive vehicles

There are a variety of FPGA based TDC architectures possible to attain the constant performance and the best TDC resolution. The counter-based architecture, the VDL technique [10], multiple interpolation approach [11], the wave union method [12] and the pulse-shrinking method [13] were effectively implemented and recognized in FPGA devices. Min Zhang[14] proposed a FPGA based TDC which comprises of a measurement matrix with resolution of 7.4ps,Alessandro Tontini[15]implemented area efficient tapped delay line based TDC in a low cost Spartan 6 device. He implemented a tap filtering technique to get improved Differential Non-Linearity (DNL) of the single delay line while keeping a good LSB value of 25.57 ps. Min zhang[16] proposed a Digital-to-Time Converter (DTC) based on the principle of quantified phase shift resolution (QPSR) is realized by examining the phase association between two periodic signals, implemented on Xilinx Virtex-5 and Virtex- 6 FPGA devices. The resolution of the DTC in on Virtex-5 FPGA is 27.1 ps and on vertex -6 FPGA is 3.96ps.M. Maamoun [17] implemented a TDC on Spartan 3E device with automatic calibration method to obtain an accurate result and to reduce the temperature dependency. In this paper, we proposed a low power TDC architecture that can be implemented in a low-cost Spartan 3E device.

II. Principle of The Proposed TDC Architecture.

The proposed work includes a coarse TDC using gray counter as the first stage TDC to reduce power consumption instead of binary counter. In binary system the probability of switching the signals are more. For instance, for a change from 3 to 4(011 to 100) all bits are inverting, it creates the delay, because of switching all signal, but this is not the case in gray code, only one bit is changing. For a change from 3 to 4,here we can observe changing of bits are very less.

The proposed two-dimensional TDC is implemented using Gray counter and an array of D Flipflops. Hence the first stage includes a gray code counter and the second stage includes a matrix of D Flipflops which provide a fine interpolation. The output is obtained as a Binary Value. The schematic diagram of Two dimensional TDC is as shown in Figure 2.

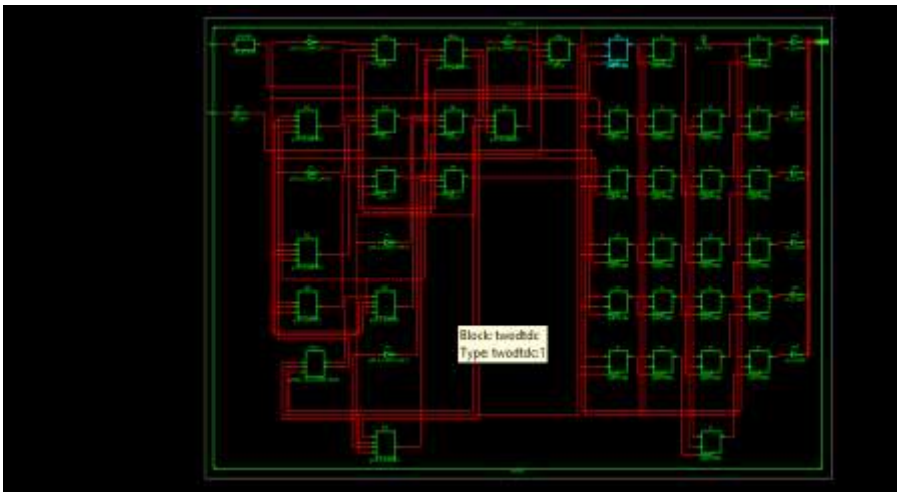

Figure 2. Schematic Diagram of Two Dimensional TDC

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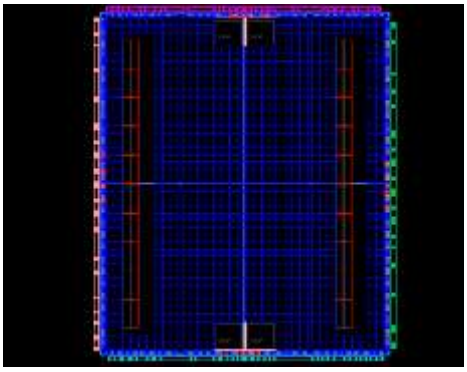
The plan Ahead tool used to obtain the device implementation of Two Dimensional TDC is as shown in Figure 3.
Figure 3. Device implementation Of Two Dimensional TDC.



The elaborated RTL schematic of Two Dimensional TDC is shown in Figure 4.

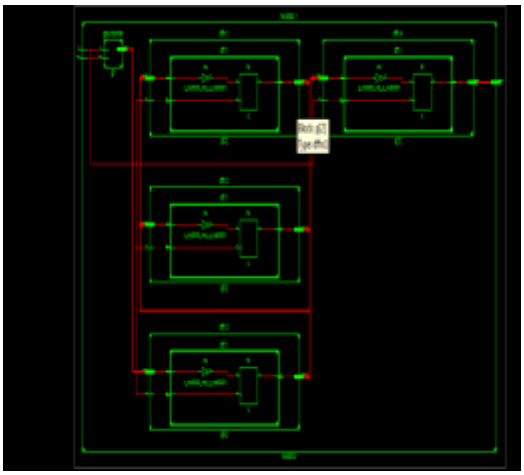


Figure 4. RTL schematic Of Two Dimensional TDC.

The input-output waveform of Two Dimensional TDC is obtained by having enable, clock, data(d) and reset as input. The simulation waveform of the corresponding Two Dimensional TDC is shown in Figure 5.

Figure 5. Simulation Waveforms 2D TDC.

III.RESULTS AND DISCUSSIONS

The Logic Utilization of TDC is evaluated based on number of LUT's used, the number of IO buffer used and the number of slices and is tabulated as in Table1.The Estimated power is calculated using Xilinx Power Estimator (XPE) for two different temperatures with different frequencies which is shown in Figure 6.

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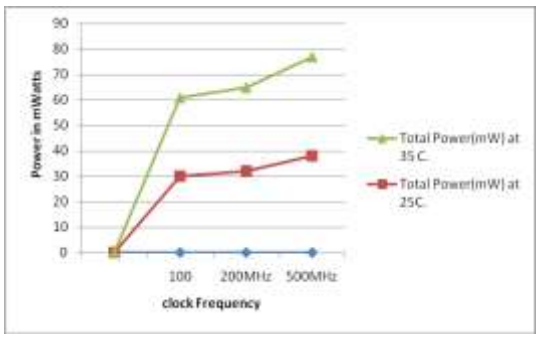

Figure 6:Total estimated power at 25^0C and 35^0C with varying frequencies.

Table 1. Logic Utilization of TDC Architecture.

LOGIC UTILIZATION		**TWO DIMENSIONAL TDC**
No Of Slices	Used	20
	AVAILABLE	768
	UTILIZATION	2%
No Of Slice Flipflops	Used	34
	AVAILABLE	1536
	UTILIZATION	2%
No Of Input LUTs	Used	32
	AVAILABLE	1536
	UTILIZATION	2%
No Of Bonded IOBs	USED	37
	AVAILABLE	63
	UTILIZATION	58%
No Of GCLKs	USED	1
	AVAILABLE	8
	UTILIZATION	12%

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We also compared our TDC architecture with the recent published results which are shown in Table 2.

Table 2: Comparison of our FPGA based TDC architectures with published results

AUTHOR	METHOD	PROCESS FAMILY	INL (LSB)	DNL (LSB)	DR (ns)	AREA	NO. OF LUTS/ FFs	CLOCK FREQUENCY (MHz)	RESOLUTION (ps)	POWER (mWatt)
Yuta Sano [18]	fine time counters	Kintex-7	_	0.06 –0.14	1.842	_	_	110	0.08–0.10	10
MinZhang[14]	Matrix of counters	Xilinx Virtex-5	–1.52 to 1.57	−0.74 to +0.7	0.5–13.5	8 × 128	666/-	135.5	7.4	0.0554
Alessandro Tontini [15]	tapped delay line	XilinxSpartan 6 device	−0.755 ÷ 0.872	−0.072 ÷ 0.070		415/2278(slices)		230	26	131
MIN ZHANG [16]	Phase difference	Xilinx Virtex-5	-0.387~ +0.171	-0.269 ~+0.247	0.005	_	2/145	75	27.1	221
MIN ZHANG [16]	Phase difference	Xilinx Virtex-6	-2.6093~ +2.4754	-0.327 ~+0.358	0.005		2/199	500	3.93	196
This work	2D TDC	Xilinx Spartan 3E	-	-	0.5	20 slices	32/34	500	15.63	40

IV.CONCLUSION

We have implemented gray code based counter as the first stage TDC to reduce power with matrices of D Flipflops as a second stage interpolator to provide fine interpolation. We analysed our TDC architecture by considering the number of LUT's used, the number of IO buffer used and the number of slices used. The estimated power of our architecture is 40mw for a bin size of 5, and also, we obtained a resolution of 15.63 ps for a dynamic range of 500ps. In future, we can include code density analysis to improve the linearity of our architecture.

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