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MODULAR MULTILEVEL CONVERTER BIPOLAR HVDC WITH SVPWM BASED VOLTAGE DROOP CONTROLLER

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ABSTRACT: The main aim of this paper is the voltage drop controller with SVPWM-based Hybrid MMC Bipolar HVDC. The hybrid boost MMC HV pulse generator with (m-0.5) nh: nh (Full Bridge-SMs: Half Bridge-SMS) has been presented in each arm to generate bipolar pulsed output voltage with voltage magnitude (+ /-mVdc, where m=1,2, ... etc) operates at greater magnitude than traditional. The proposed, controlled droop, Modular Multilevel Converter (MMC) with Half-Bridge Sub-Modules will further improve system performance. That is, the dynamic conduct of the Network is growing. By integrating the modulation Space Vector Pulse Width (SVPWM) with MMC HVDC, the number of switches can be reduced, and the losses and power factor increased. For the proposed approach simulation models are built using the Matlab / Simulink framework for different ratios of Full Bridge-SMs to Half Bridge-SMs.

Keywords: Pulse generator, Pulsed power system, SVPWM

I. INTRODUCTION

The bipolar high voltage pulse generators[1]–[3] are the most widely used generators in various power system applications. Number of methods are applied to generate the bipolar HV pulses[1]–[11]. The standard technique is for the HVDC power supply to be combined via the VSI (voltage source inverter). About Chart1. High voltage switches are executed via a series of connected semiconductors. It is important to inject dynamic voltage distribution into the flourishing operation of the series of connected devices by controlling the pulse of the gate[12], the process was very complex. Parallel to this, the dual cascade H-bridge inverter with isolated voltage was used[1]. Stage by stage H-bridge performed multi-tasks to feed pulsed load, which are sequentially connected in this article. The Multi Cascaded H-bridge needs external source of insulated voltage, that's the big drawback. By using the High Voltage H-bridge Marx-generator at load improves system accuracy[2],[5] the H-bridge 's static voltage sharing and dynamic voltage sharing is achieved via the connected inverter collection, with this system conversion increase. High voltage bipolar pulse generator based on the push-pull inverter is suggested in [6] and [7], which are desired at the output.
Consistent voltage distribution in connected semi-conductor system method series is proposed in[13]. In [8]-[11], solid-state Marx topologies are proposed for the generation of bipolar pulses and unipolar pulses, and a large number of parallel semiconductor devices are important. High Voltage switch series connected devices are replaced with the proposed modular solid-state switch in[9]. For preserving the voltage rating and minimizing the number of High Voltage device components, modular switched capacitor pulse generators were prearranged with condenser-diode voltage multipliers. The output pulses of the High Voltage Pulses Generator are unipolar. It generates bipolar pulses by varying the charge of the H-bridge high voltage. In high voltage system voltage source[16], the scalability and modularity of the Inverter Multilevel Modular Converter (MMC) is considered in. With comparatively low voltage semiconductor, there is no need in MMC systems to generate HV output pulses for the connected devices in sequence.

A hybrid boost MMC HV pulse generator was proposed in this paper, here in this MMC each arm has a FB-SMs (Full-Bridge SMs) along with HB-SMs(Half- Bridge SMs) by a ratio of (*m*-0.5) n_h: n_h, where as n_h was the number of the Half- Bridge SMs per arm and '*m*' as the boosting factor, i.e., equal to ratio of output pulse voltage magnitude and DC voltage input. To generate pulsed output voltage of(V_{dc}, $2V_{dc}$,$3V_{dc}$…etc.) boosting factor '*m'* integer (1, 2,3…etc.) should be defined respectively. In the proposed system each arm of Full-Bridge SMs and Half- Bridge SMs of hybrid boost MMC-HV pulse generator is rated as $\frac{V_{dc}}{n_h}$. The magnitude $\frac{+}{-}mV_{dc}$, of the generated bipolar pulsed output voltage of the proposed system is greater than output voltage of conventional MMC pulse generator, by

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the Half- Bridge SMs, by magnitude $\pm -0.5V_{dc}$. By this the proposed design of MMCHV pulse generator affords boosted output voltage by utilizing low voltage semiconductor devices. By this, each arm has been controlled to generate boosted output voltage.

In MMC to maintain the capacitor voltages constant is the major task, by this different techniques of capacitor voltage balancing are done in this paper, mostly sensor-less balancing technique and conventional sensor technique [16]. Here, detail frame work of the proposed system and mathematical analysis is presented in this paper.

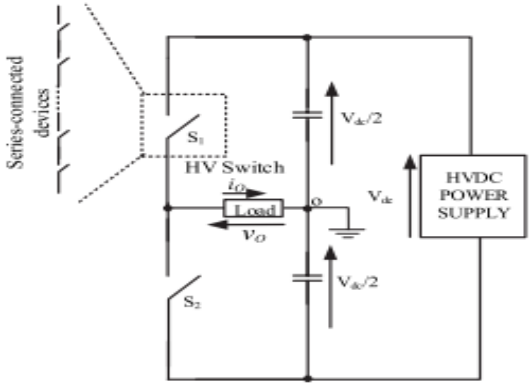
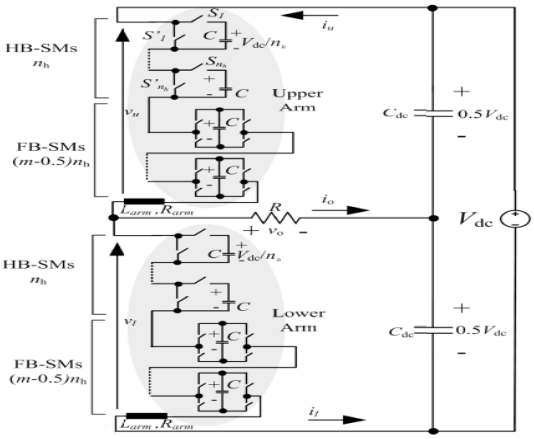


Fig. 1. Bipolar Conventional HV pulse generator

II. PROPOSED HYBRID BOOST MMC BASED HV PULSE GENERATOR

In this proposed method high voltage pulse generator, based on the MMC hybrid boost, is shown in Figure 2. Any arm contains Full-Bridge SMs and Half- Bridge SMs by a ratio of $(m-0.5)n_h : n_h$, correspondingly. Each SM (Full-Bridge SMs and Half- Bridge SMs) is classified as $\frac{V_{dc}}{n_h}$; where n_h is an equal number, reflecting number of Half- Bridge SMs per arm. Whereas, '*m*' was boosting component, here the integer value greater than the zero, ratio in between output magnitude and DC voltage input is represented as $DC\ (m = \frac{V_p}{V_{dc}})$; where V_p is peak output voltage (V_0).

Here, number of SMs complete was $(m-0.5)n_h$ per arm. As shown in Fig3 and Fig4 respectively for Half- Bridge SMs & Full-Bridge SMs, Half- Bridge-SM had positive voltage state and zero voltage states while Full-Bridge-SM has positive voltage state, negative voltage state and zero voltage states.



(a)

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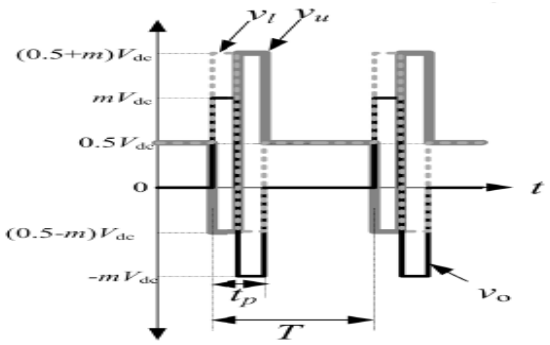


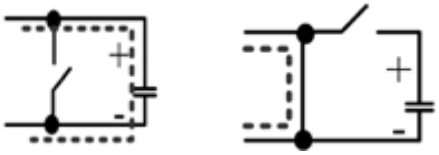
(b)

Fig2. Hybrid boost MMC HV pulse generator of the proposed system. (a) configuration, (b) variation of the upper arm voltages, lower arm voltages, and output operation.

In fig1. at load terminal (V_0) by controlling the upper arm voltage and lower arm voltages the bipolar output voltage pulse are generated. $(0.5-m)V_{dc}$ and$(0.5+m)V_{dc}$ are the voltage magnitude ranges of the arm, and $\pm mV_{dc}$ is the magnitude of the output voltage pulse.

Appropriate Half- Bridge SMs and Full-Bridge SMs should be able to operate in a positive pulse when generating positive arm voltage is necessary, and other SMs in similar arm will be avoided by operating at zero state. The choice of SMs concerned here is focused on the technique of condenser voltage balancing implemented to ensure efficient operation by controlled capacitor voltages.

The following section will demonstrate various voltage balancing techniques for the proposed system, i.e., sensor techniques and sensor-less techniques.



(a) (b)

Fig 3. Voltage states of Half Bridge-SMs. (a) positive voltage and (b) zero voltage states.

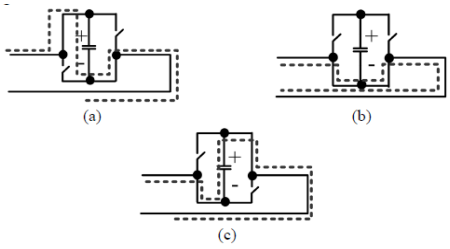


Fig 4. Full Bridge-SMs Voltage states . (a) positive voltage (b) zero voltage and (c) negative voltage states.

In the fig2. two +voltage states of arm voltages are shown that are $0.5V_{dc}$ &$(0.5+m)V_{dc}$. At first stage voltage magnitude is $0.5V_{dc}$, $0.5n_h$ away of $(0.5+m)n_h$ SMs for each arm, need to be concerned of its current direction by the +voltage level. In zero voltage state operation the mn_h SMs of the same arm need to be cross over. The controlling of the MMC HV pulse generator is pedestal on capacitor voltage balancing. During another voltage state operation $(0.5+m)V_{dc}$, all Half- Bridge SMs and Full-Bridge SMs of arm has been operated, those are need to in +voltage level only. All Full-Bridge SMs of the arm need to be operate in -voltage level to ensure the -voltage which contains the path current, in other case Half- Bridge SMs of the same arm need to be cross over the operation in zero voltage level.

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III. PROPOSED SVPWM TECHNIQUE

Space Vector PWM generation module makes modulation index commands for each PWM loop and generates the correct gate drive waveforms. This section explains how to run and configure SVPWM modules.

A 3-phase 2-level inverter with configuration of a DC connection may contain the 8-possible switching states that generate an inverter voltage output. Here, the switching state of an inverter produces the Space Vector voltage (active vectors $V_1, V_2, V_3, V_4, V_5, V_6$ zero voltage(V_0) vectors V_7 & V_8) inside Space Vector plane. The active vector ($V_1, V_2, V_3, V_4, V_5, V_6$) was $\frac{2}{3} V_{dc}$ (voltage DC system) magnitude.

Space Vector PWM (SVPWM) module, was exposed in the Fig, inputs modulation index commands (U_α, U_β) which are orthogonal signals (α, β). The Benefit function of the SVPWM module was exposed in the Fig. A Vertical axis of fig represents an usual peak motor phase voltage ($\frac{V}{V_{dc}}$), and horizontal axis was standardized modulation index (M).

Following equation can approximate the fundamental line-to - line inverter RMS output voltage (V_{line}):

$$Vline = Umag * Mod\_Scl * Vdc / \sqrt{6} / 2^{25} \quad \text{..... (1)}$$

Where DC system voltages (V_{dc}) are in volts

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Maximum achievable modulation ($U_{mag}L$) within linear operating range is given by:

$$Umag\_L = 2^{25} * \sqrt{3} / Mod\_Scl \quad \text{..... (2)}$$

Modulation above transpires with modulation of $U_{mag} > U_{mag}L$. This applies to case where voltage vector under increases beyond boundary of a hexagons. Under these conditions Space Vector PWM algorithm can rescale within a Hexagon limits magnitude of a voltage vector to fit. Magnitude of voltage vector inside a Hexagon is reduced but a phase angle is still maintained. In field of over modulation, transfer gain of a PWM modulator decreases and becomes nonlinear..

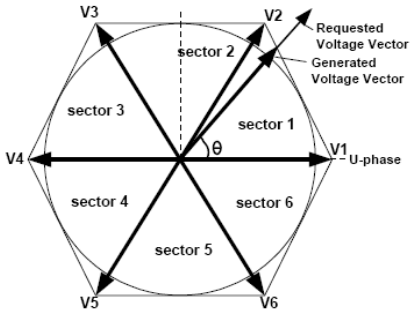

Fig:5 Rescaling of Voltage Vector

Upon issuance of a modulation index commands (U_{alpha} and U_{beta}), a sub-module SVPWM T_m starts its calculations at a rising edge of PWM Load signal. SVPWM T_m module implements the algorithm that selects an active space vectors ($V_1, V_2, V_3, V_4, V_5, V_6$) being utilized and decides correct time period $w.r.t$ one PWM pulse for each active vector. Also chosen vectors which are assigned to zero. SVPWM T_m module usually consumes 11 clock cycles and 35 clock cycles in over modulation cases falling edge of n_{SYNC} is readily available with the novel set of

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Space Vector times and the vectors for real PWM generation (U_{Phase}, V_{Phase}, W_{Phase}) by Generation Sub-modul. Until the edge of the nSYNC signal dropped, at least 35 clock cycles of load had to be activated; otherwise new modulation commands would not be implemented early. PWM waveforms for voltage vector located in the Space Vector plane Fig6 and Fig7 are shown in the above voltage vector rescaling figures. Gating pattern outputs (...) include the application of dead-times

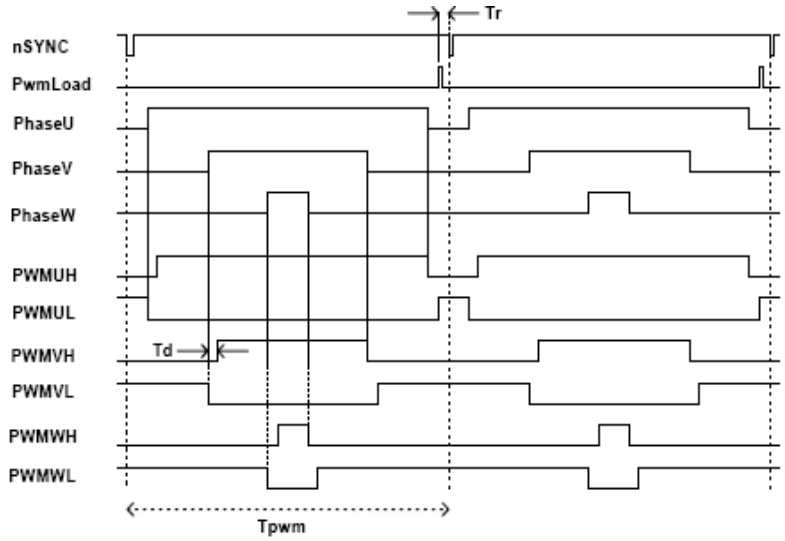

Fig.6 Space Vector PWM of 3-phase

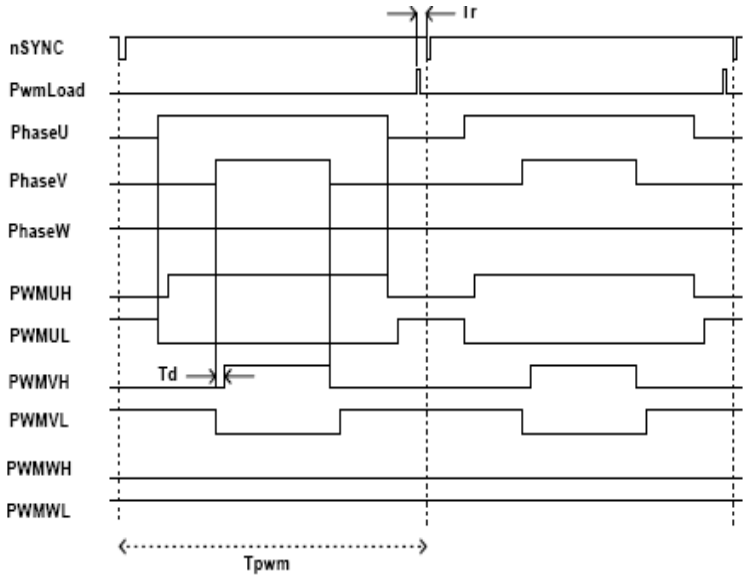

Fig.7 Space Vector PWM of 2-phase (6-step PWM)

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II. SIMULATION RESULTS

A) EXISTING RESULTS

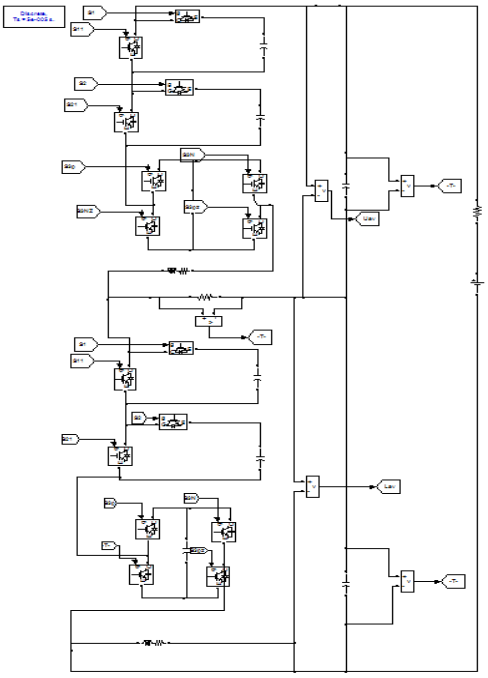

Fig 8. Hybrid boost MMC based high voltage pulse generator of the proposed system

CASE 1 $(M = 1 \; and \; n_h = 2)$

The corresponding simulation results are shown in Figure 6 and Figures 6a and 6b show the variation of upper and lower arm voltages with the operation. Figure 6c shows the pulsed output voltage with a magnitude of +/-V dc (as m=1).

It is clear that a pulsed output voltage with desired pulse width, rise time, and magnitude has been generated successfully, while keeping the capacitors' voltages balancing as shown in Figure 6d.

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It is clear that a pulsed output voltage with desired pulse width, rise time, and magnitude has been generated successfully, while keeping the capacitors' voltages balancing as shown in Figure 6d.

In case1, corresponding simulation results, Fig 9-12 and Fig 9 and Fig 10 exposes difference of upper arm voltages and lower arm voltages with action. Figure 11 indicates pulsed output voltage of $\pm 20kV \; (asm = 1)$. It was obvious that the pulsed output voltage with desired pulse duration, the magnitude and time increase was generated effectively, while maintaining condenser voltages in balance as exposed in Fig12

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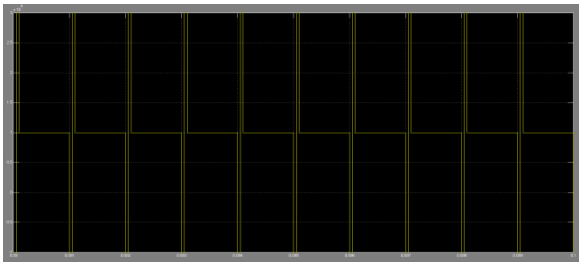

Fig.9 Voltage of Upper arm

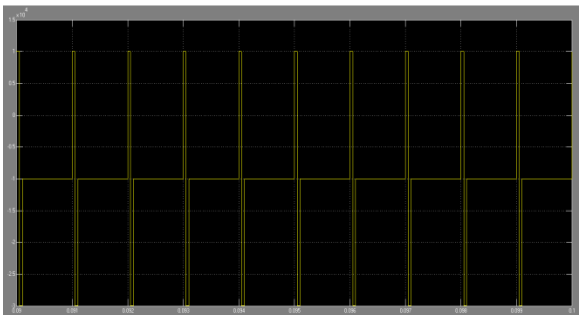

Fig.10 Voltage of Lower arm

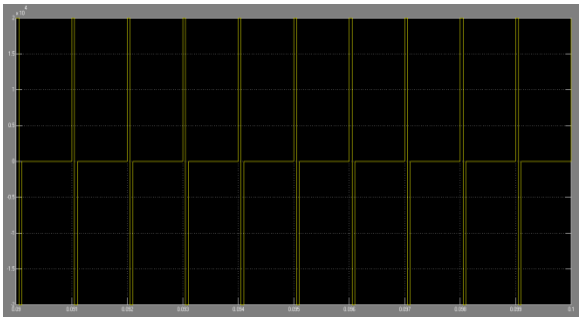

Fig.11 Voltage of Pulsed output (+/- 20kV)

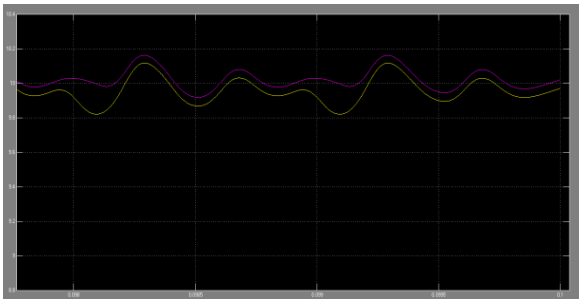

Fig.12 Voltage of SMs' capacitors

CASE 2$(M = 2 \; and \; n_h = 2)$

The corresponding simulation results are shown in Figure 7. It is clear that the desired pulsed output has been generated successfully (Figure 7c) with magnitude of +/- 40 kV with 20 kV dc source (as m=2) while keeping the capacitors' voltages balancing as shown in Figure 7d.

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Figures 13-16 shows the outcomes of the associated simulation. It was obvious that desired pulsed output (Fig15) was successfully achieved with the magnitude of $\pm 40kV$. with a source of $\pm 20k\,V_{dc}\,(asm = 2)$, while supervision condenser voltages in balance as exposed in Fig16

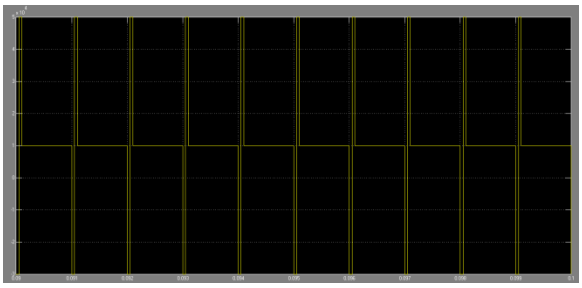

Fig.13 Voltage of Upper arm

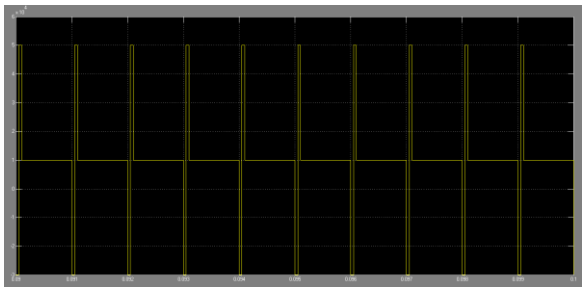

Fig.14 Voltage of Lower arm

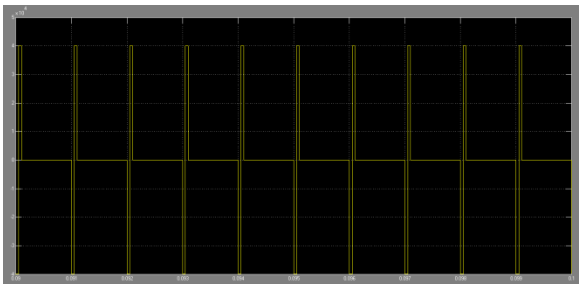

Fig.15 Voltage of Pulsed output (+/- 40kV)

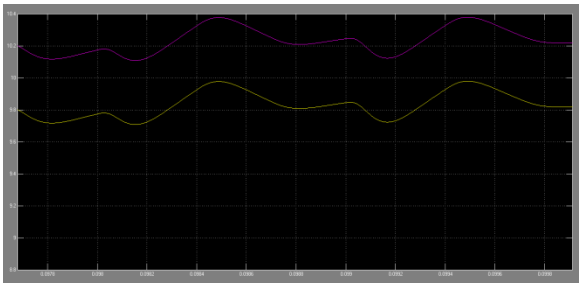

Fig.16 Voltage of SMs' capacitors

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B) EXTENSION RESULTS

CASE 1$(M = 1 \ and \ n_h = 2)$

In case1, respective simulation results are exposed in Fig17- Fig 19 and Fig17 and Fig 18 display difference with upper arm voltage and lower-arm voltage operation. Fig12 exposes pulsed $\pm 25kV$ output voltage that can be enhanced relative to current results $(asm = 1)$. It is obvious that a pulsed output voltage with desired pulse length, magnitude and time increase has generated effectively

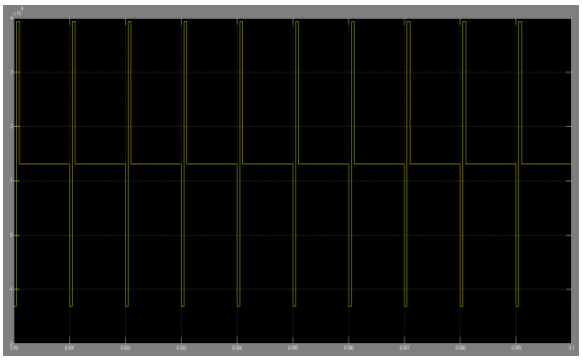

Fig.17 Voltage of Upper arm

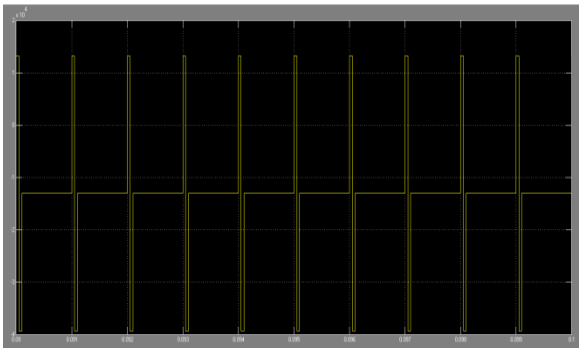

Fig.18 Voltage of Lower arm

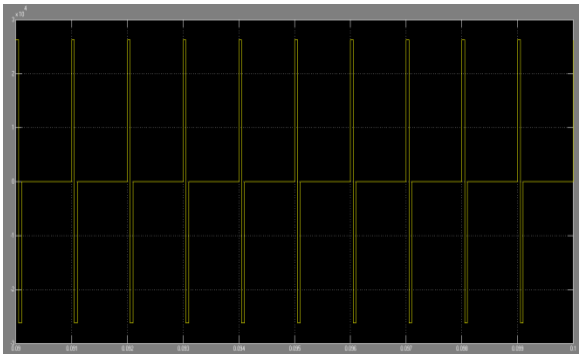

Fig.19 Voltage of Pulsed output (+/- 25kV)

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CASE 2 $(M = 2 \; and \; n_h = 2)$

The simulation results are illustrated in Figures 20-24. It is clear that the desired pulsed output with a magnitude of $\pm 50kV$ with a source of $20kV_{dc}\,(asm = 2)$ was successfully achieved (Fig15), while supervision condenser voltages in balance as shown in Fig24. Figure 24 clearly exposes smooth wave form compared to current method due to SVPWM control strategy

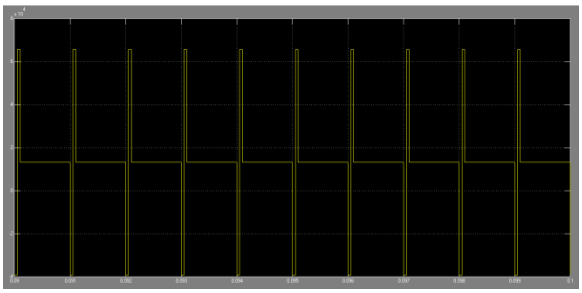

Fig.20 Voltage of Upper arm

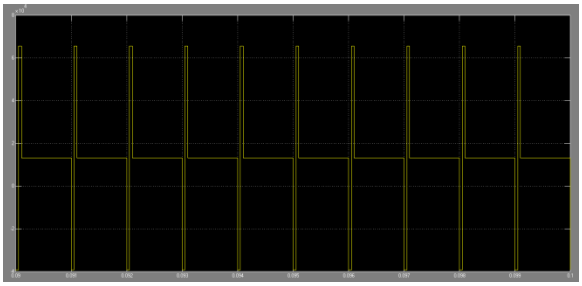

Fig.21 Voltage of Lower arm

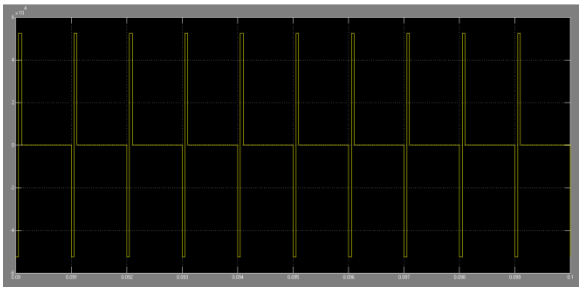

Fig.22 Voltage of Pulsed output (+/- 50kV)

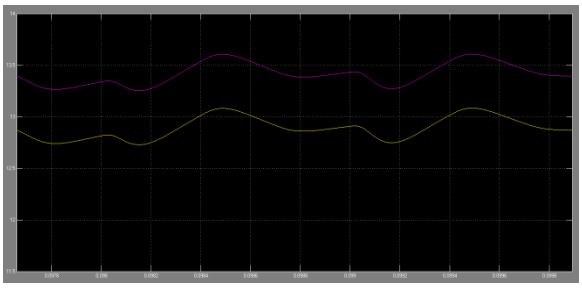

Fig.23 Voltage of SMs' capacitors

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CONCLUSION

This project proposes topologies based on SVPWM-based Pulse Generator (PG) based control electronic devices and modular multilevel converter submodules. The proposed topologies are divided into two main classes, namely: PGs fed from a supply of HV DC and PGs fed from an LV DC supply. The first group presents a new family of HV DC fed topologies that improve the performance of existing HV DC fed PGs, such as the generation of versatile pulse-waveforms and the full use of DC connection voltage. The second group is dedicated to a new family of LV DC-fed PG topologies with flexible pulse-waveform generation, controlled operating output, and high tension gain. All the proposed SVPWM based PG topologies share the important aspect of modularity in the newly developed HV PGs that delivers redundancy and robust pulse generation operation.

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