

LOW-POWER AND LEAKAGE REDUCTION IN 10T SRAM USING TANNER EDA

R. Jegadeeswari¹, Ramyajothikumar², M. Mukila³, P Raja⁴

^{1,3}Student, ²Professor, ⁴Head of the department

^{1,2,3,4}Department of Electronics and Communication Engineering

^{1,2,3,4}Sri Manakula Vinayagar Engineering College, Puducherry, India

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Abstract

In recent times, SRAM plays an important role in battery motorized movable devices and low authority sensor presentations. In existing system, the 10T SRAM bit cells with 32nm CMOS delivers features of high density and fast performance with less number of transistors for memory design, but it still suffer from low array efficiency, read disturb issues and high energy per access. The proposed system, delivers three repetition of process (different read port) of SRAM bit cells which is based on only nMOS in read port to reduce data dependent read port leakage as well as with 10T SRAM designed with 512 bit cells. The proposed system is implemented in Tanner EDA with 22nm CMOS Machinery with resource power of 80mV then also proved the comparison in relations of area plus power.

Keywords-- tanner EDA, leakage, portable devices, data dependent.

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INTRODUCTION

In VLSI, the procedure used to design a circuit by stuffing more reasoning devices in a minor zone. This circuit now use the sheet furls so that it can be designed in minor area of limited millimeters. It remains universally in many processor, automobiles, etc. In order to build a circuit it required a lot of skill in various frontages in similar content, we will discuss this in future sectors.

Dealing with VLSI Circuits

The way that blocks identical type latches wear implemented in various methods. However the method varies the outcome will be similar.

Circuit Delays

Enormous amount of complex devices are run at very high frequencies has only one challenge that is propagation delay in signal which is caused from gates, wire, etc. Because of the enormous speed the delays added to the devices and it is converted to analog to clock speed.

Power

The power consumption is improved by adding the effect high frequency operations. The high power dissipation and the device consume battery power soon are two portable device result. The reduced surface area and heat carriages are combining to form a threat to static devices.

Layout

The task to position the apparatuses is common to every branch in the electronics. There are numerous possible procedures such as, multiple layers of dissimilar resources on single silicon, dissimilar arrangements of minor part in the same elements and so on. Fabrication of the VLSI chip is disturbed by layout; tricky in implementing elements in silicon or stress free industrialized.

Electronic Design Automation

In EDA enormous amount of tools available for reproduction, operation and combination circuit using VHDL. There few tools which are all ordered as vendor's plan suite such as Altera's Quartus II or Xilinx's ISE. Some other design suits tools are also provided by EDA such as Leonardo spectrum, Model Sim and Simplify. The proposal in the manuscript is moreover specified as

Altera or Xilinx. The tools utilized were either ISE together with MaxPlus II, ModelSim mutually advanced.

SRAM inhabits an important allocation in system-on-chip (SoC). In SoC the SRAM has a well-known influence in complete power consumption. In order to allocate the peripheral circuitry memorial strategy engineers allows to residence as many as cells possible per column, area is a momentous factor in circuit designing. The 6T and 8T conventional cells are unqualified to work in lengthy columns. This is cause by the data dependency leakage and voltage swing in read bit line by placing many cells in a single column. Hence, we have to design a new model to overcome this issue. In preceding methodologies [1]-[3] have tried to overcome this issue my refining the ION/IOFF ratio to allow 1k cells per column. Even though it shows as improvement in this design but it still suffered by data dependent leakage or it need huge area problem.

SRAM's influence has developed an important arrival of transportable device which is powered by battery and low power radar proposals. Supreme SRAM proposal have been fixed to smooth voltage escalating and enlightening harvest. Conservatively accomplished 6T in SRAM certificate the high compactness, bit enclosing, fast incongruity distinguishing which is suffered by hail-select solidity, dependability in read disturb and incompatible in encrypt and decrypt sizing.

In order to diminish the SRAM's read bit disturb and half select by optimizing the word line voltage and it also included the word line drive under assists by corner tracing method [4] or by using entrée transistor [5]. To establish a trade-off among write ability and read stability by delaying the word line enhancement [6] to equalize the inner voltage of half select cells. Execution of negative cell GND [7] improves the read stability but it causes high voltage budget for grounding several rails [8].

To evolve the read stability we have to use regulator in order to reduce the precharge voltage about 70% of source voltage [9]. Disturb problem can be reduced by using the above mentioned method to access transistors. On the other hand bit line can precharge by an Nmos and not by Pmos to gain single VTH fall on bit line [10]. By using selective precharge method [11] used to reduce the voltage of bit line by dividing so then the half select

problem will be improve. In [12] they proposed a dynamic power supply technique in column, by using this method write, read and standard modes which relive half select problem and allow bit enclosing. To advance half select strength they used a cross point collection of word in rows and columns [13], [14]. Minor bit -line also recycled to progress the read strength. Here they enlightened the dynamic read sheet and reduced the capacitance of bit line. Array architecture above 12% was implemented to address half select problem by decoupling huge bit line with capacitance from cells [15]. Easy errors includes SBU which is single bit upset and MCU as multiple cell upset are all obtained by the bombardment of huge cosmic energy or alpha particle or thermal neutron [16]. For each 10% reduced in voltage supply increases 18% of soft error in cells [17]. There I a problem for low voltage level SRAM's because sub threshold region, leads to critically energized nodes reduces the frequency of MCU's [18]. ECC's interleaving arrangement bit is combined with diminished MCU's [19] and [20]. By using both column and row word lines we can remove half select and disturb in column decoupled 8T [21], free disturbance in 9T, multiple port disturb reduced in 9T cell [22], and also in differential design of 10T cells.

The paper is made-up of follows sections such as Section 2 defines the proposed model section 3 includes the result and working and also the comparison in term of area and power with existing models. Section 4 concludes the model.

PROPOSED

10T SRAM Cell with Contribution

The irreplaceable S-10T SRAM cells of upcoming bit is shown in Fig.1. The 4T transistor read port is constructed by an inverter and then the transistor gate (TG) which is added to 6T transistor, it separate the read terminal from interior memory nodes. The inverter M6 and M7 which is activated by the node call QB and the RBL is also drive by the node through TG which is M8 and M9 it is controlled by two harmonizing WLs. During read operation the S-10T is fully discharged or charged by RBL so it is fully pointless to arrange a precharge for RBL. When the rad data varies then the dynamic power is disbursed on RBL. When the consecutive "0"s or "1"s are readied out then the dynamic power dissipation will be zero in RBL. This above feature is more suitable for image or video processing because in image data they have exceptional relationship and also identical read out in cycles. Regrettably, in 6T write performance is initiated in column select array in writing, so the unselected row are perform the dummy read out in WL and then undergo read actions while writing, this action is denoted as a read disturb error occurs in 6T. So, it is not qualified for the enclosing architecture. Because of TG more power is dissipation by addition of rail-to-rail swing on RBL.

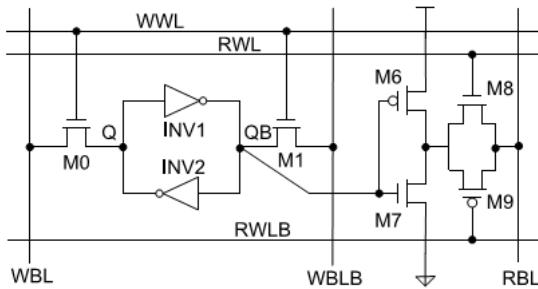


Figure 1. Schematic of Proposed 10T SRAM

In order to enable the column-select architecture we adopt terminal-share data-attentive scheme. In WL is the 6T S-10T cell is encouraged by y-direction and also in order to activate x-direction two supplementary entrée transistors such as M10 and M11 are added to 6T and undistinguishable time are energized

by corresponding write bit terminal duos are WBL and WBLB. Each and every extra transistor is communicated by end-to-end 10T in row. The row and column WL is fully ON and impartial because of the writing procedure that inscribed the data then store it in communal bit which are all via shared entrée and internal entrée transistors. From the previous SRAM over proposed bit-interleaving's are enable patterns varies and it can also interleaved in column by horizontal and vertical WLs. However, the write entrée devices communal by various bit in column, in our enterprise write entrees are communicated to two bit cell.

Bit-Interleaving and Communal Word Line Architectures:

In SRAM architecture two methods are used to align the words. The communal word lines are in Fig. 2(a) and the bit interleaving in Fig. 2(b). All bit with similar words placed next to each other in communal word architecture which is in Fig.2. Because of patience and compression and also it has end to-end bit, also the prospect of multi spineless error is high by have all this advantages this project is widely used. This architecture is used to overcome the soft error problems. The meticulous clarification of this method is explained. It is commonly used in SRAM cells, in order to protect the soft error area proficient for wiring.

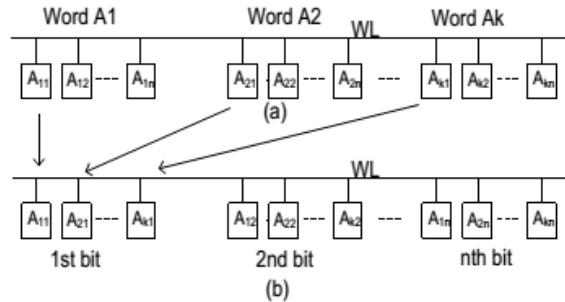


Figure 2. Architecture of Bit Interleaving

Bit line Leakage Reduction Technique

The bit terminal leakage is minus relevant on the base of magnitude associated to cell leakage; it is very significant since it disturbs the consistency of memorial device. The 10T SRAMs worst-case consequence for solo column portion. The retrieved cell "adds 1" while the others add "0". While reading the cell, bit terminal leakage power becomes a noise beside the cell power, which includes functional drop in voltage on bit terminal. The sense amp required enormous time to spot the input deviation leads to high read latency, or the power of the entrée cell is approached by leakage, it could afford fault output. In previous CMOS technology design rule are use on-off power ration higher than 10 was conventional enough to function, new enthusiastic designed with initial leakage-controlled technique.

Software requirement

Tanner operation is a Computer Study which is encoded as Analogue Combined Circuits. Tanner software tool involves,

1. Schematic (S) Edit
2. Simulation (T) Edit
3. Waveforms (W) Edit
4. Layout (L) Edit

Consuming these machine tools, zing database offers capability to project & simulate fresh designs in Analogue Combined Circuits previously to the period overriding & expensive practice of chip production.

RESULTS AND DISCUSSION

The graphical structure of proposed 10T SRAM is in Figure: 3. It has two entrée transistors such as ACL and ACR, then the cross coupled inverters such as PUL_PDL and PUR_PDR. Each cell in the read ports are all comprises of four Nmos such as R1, R2, R3 and R4. High performance, data dependence in read bit leakage are

all improved in Fig. 3(a) read port. High density, low power consumption and data independence read bit leakage are all upgraded in Fig. 3(b) and (c) read port.

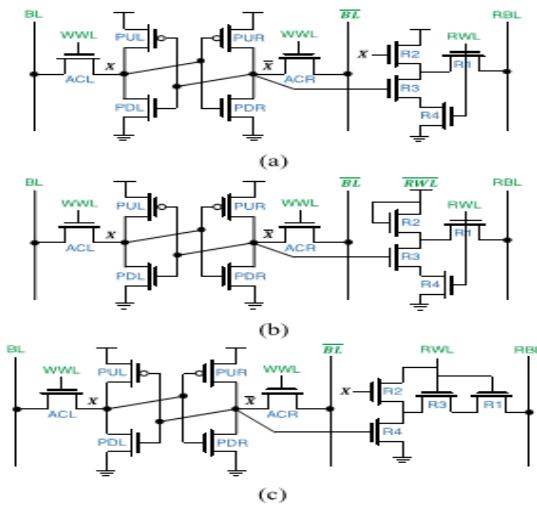


Figure 3. Proposed circuit (a) 10T_P1,(b) 10T_P3 and (c) 10T_P2

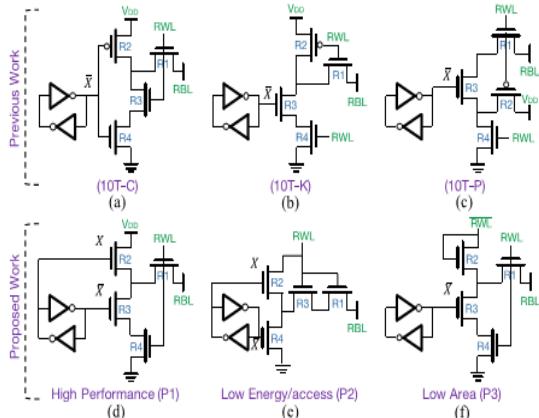


Figure 4. Proposed circuit of read port (a), (b) and (c) for previous work and (d),(e) and (f)

S-Edit output for 10T-P1 SRAM

The 10T-P1 SRAM circuit Figure: 3(a) which is designed in s-edit which is shown in Figure: 5(a).

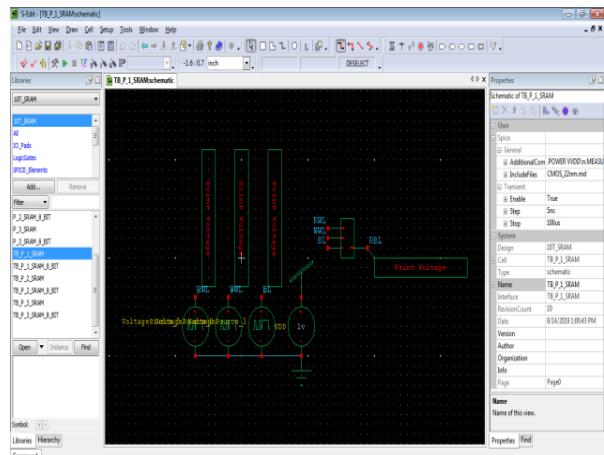
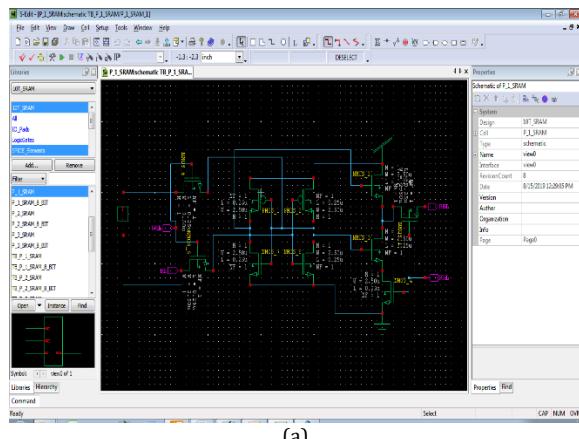


Figure 5. 10T-P1 SRAM s-edit circuit (a), (b)

W-Edit output for 10T-P1 SRAM

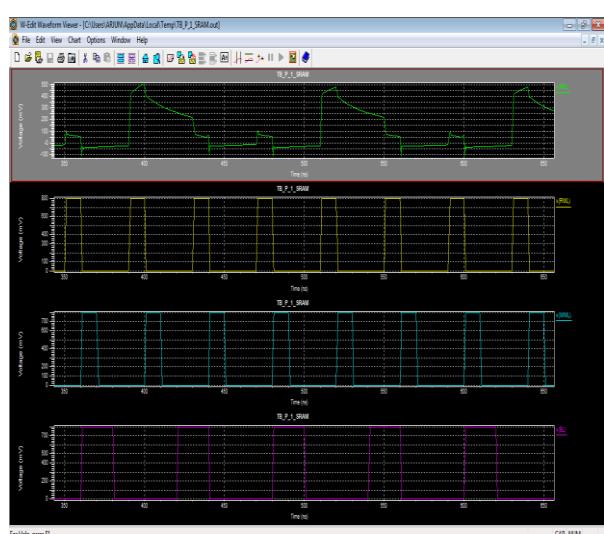
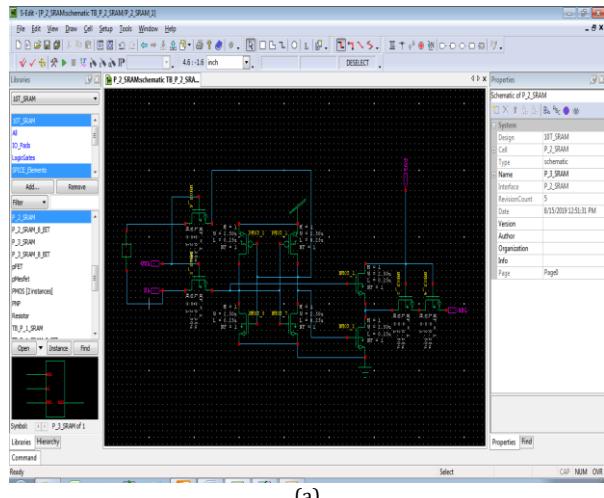


Figure 6. 10T-P1 SRAM w-edit circuit

S-Edit output for 10T-P2 SRAM

The 10T-P1 SRAM circuit Figure: 3(c) which is designed in s-edit which is shown in Figure: 7(a).



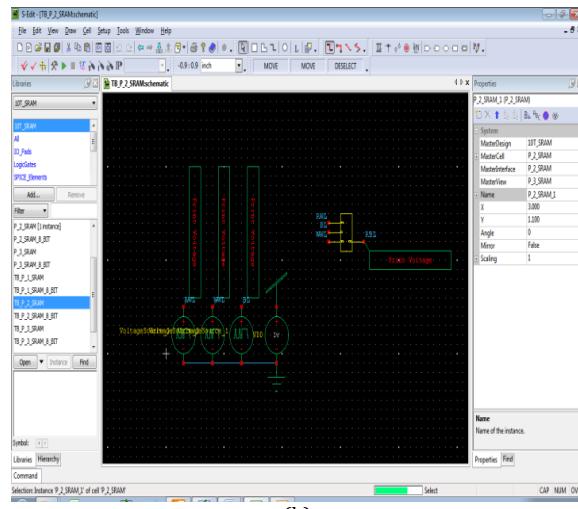


Figure 7. 10T-P2 SRAM s-edit circuit (a), (b)

W-Edit output for 10T-P2 SRAM



Figure 8. 10T-P2 SRAM w-edit circuit

S-Edit output for 10T-P3 SRAM

The 10T-P3 SRAM circuit Figure: 3(b) which is designed in s-edit which is shown in Figure:9(a).

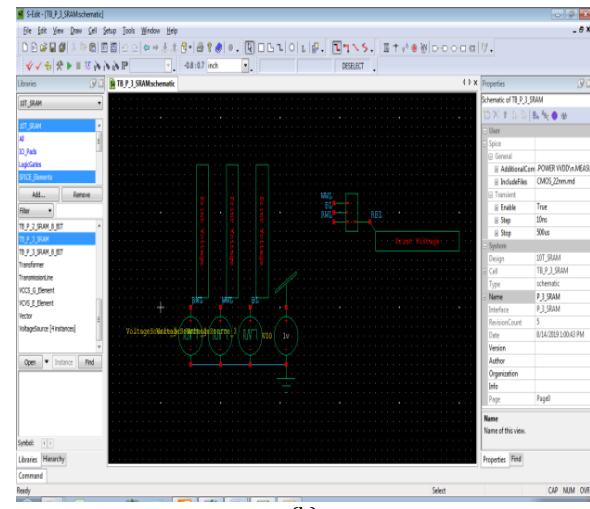
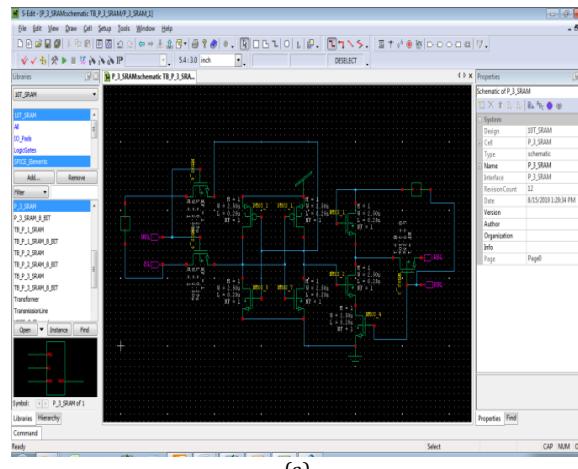


Figure 9. 10T-P3 SRAM s-edit circuit (a), (b)

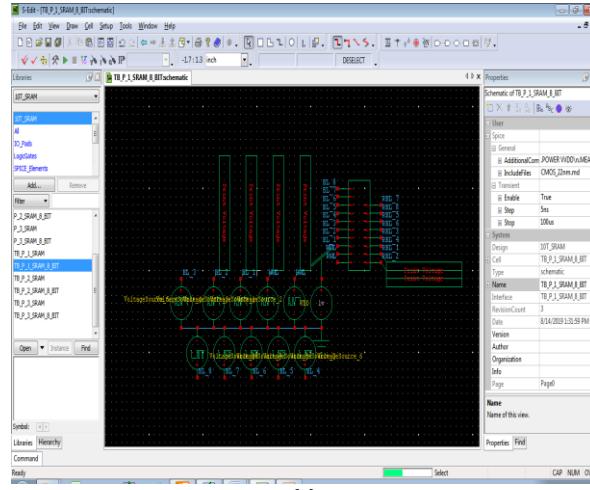
W-Edit output for 10T-P3 SRAM

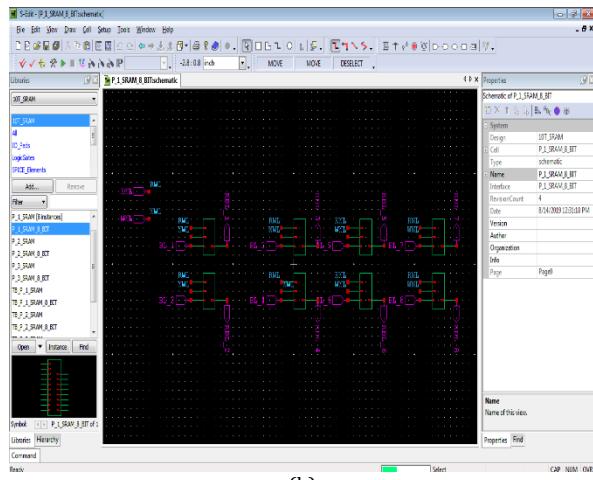


Figure 10. 10T-P3 SRAM w-edit circuit

S-Edit output of 10T-P1 SRAM using 8 bit

The 10T-P1 SRAM circuit using 8 bit, Figure: 3(a) is designed in s-edit which is in Figure: 11(a).





(b)

Figure 11. 10T-P1 SRAM using 8 bit s>Edit circuit (a), (b)

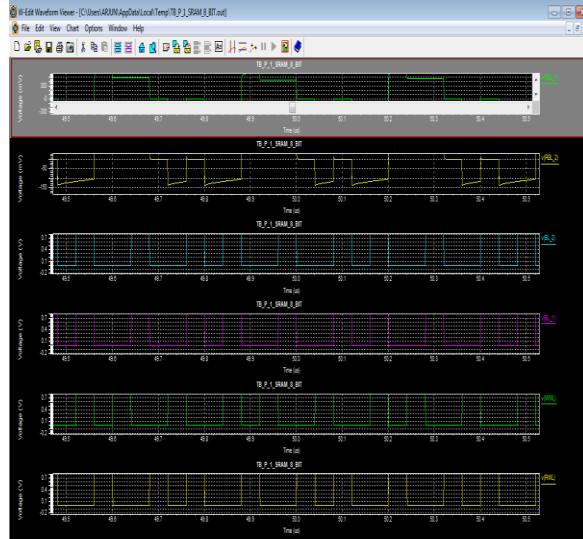
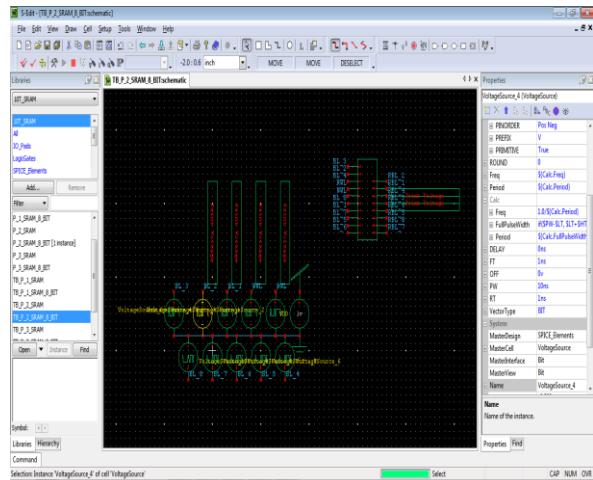
W-Edit output for 10T-P1 SRAM using 8 bit

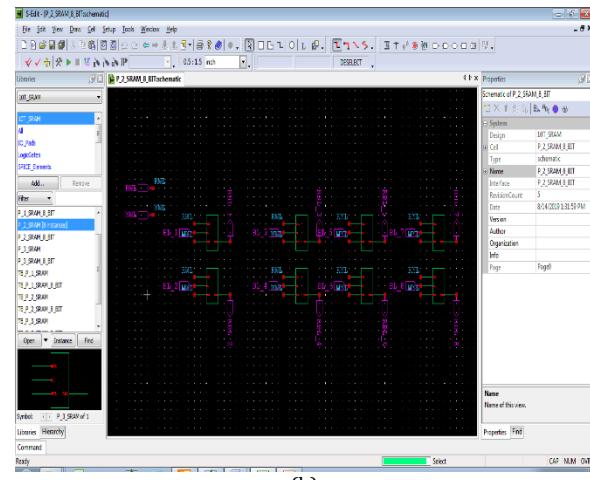
Figure 12. 10T-P1 SRAM using 8 bit w>Edit circuit

S-Edit output of 10T-P2 SRAM using 8 bit

The 10T-P2 SRAM circuit using 8 bit, Figure: 3(c) is designed in s>Edit which is shown in Figure: 13(a).



(a)



(b)

Figure 13. 10T-P2 SRAM using 8 bit s>Edit circuit (a), (b)

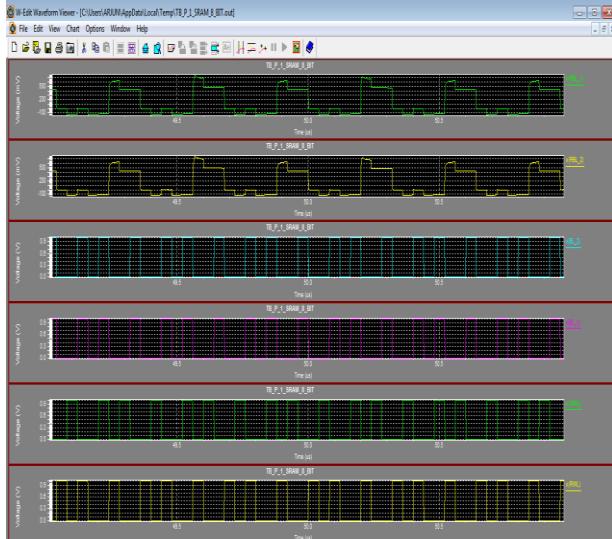
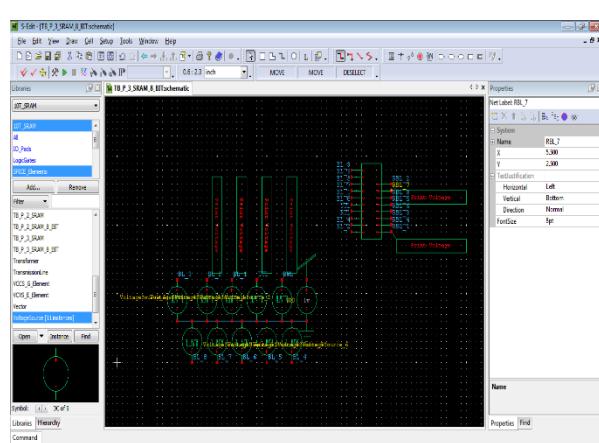
W-Edit output for 10T-P2 SRAM using 8 bit

Figure 14. 10T-P2 SRAM using 8 bit w>Edit circuit

S-Edit output of 10T-P3 SRAM using 8 bit

The 10T-P3 SRAM circuit using 8 bit, Figure: 3(b) is designed in s>Edit which is shown in Figure: 15(a).



(a)

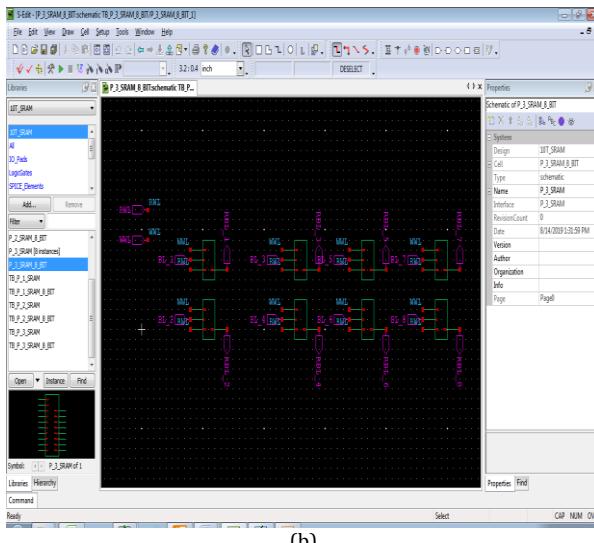


Figure 15. 10T-P3 SRAM using 8 bit s-edit circuit (a), (b)

W-Edit output for 10T-P3 SRAM using 8 bit



Figure 16. 10T-P3 SRAM using 8 bit w-edit circuit

Area and power outputs for 10T SRAM

The 10T-P1 SRAM circuit, Figure: 3(a) and there s-edit and w-edit outputs are all shown in above Figure: 5 and 6. There area and power output are shown below in Figure: 17(a), (b).

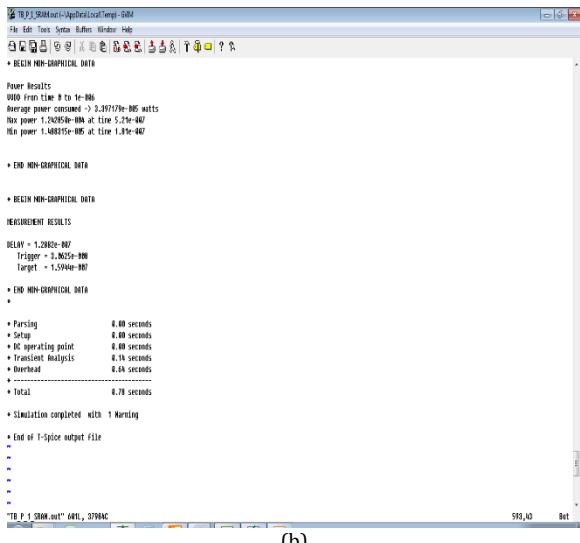
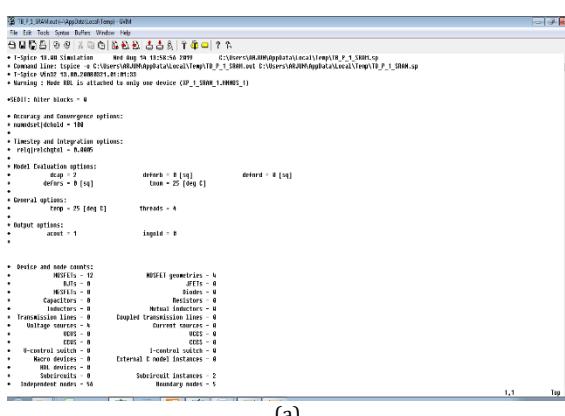
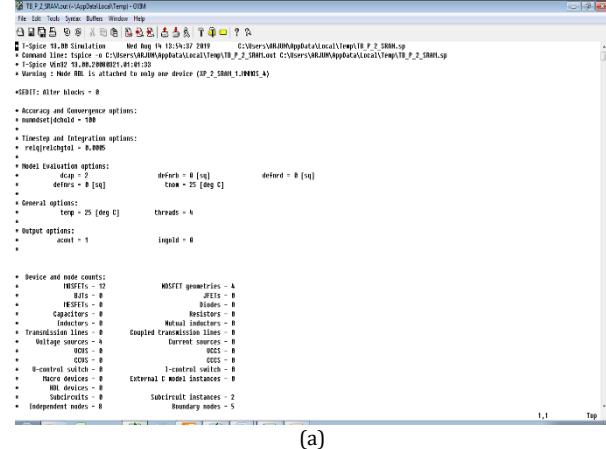


Figure 17.10T-P1 SRAM area and power output (a), (b)

The 10T-P2 SRAM circuit, Figure: 3(c) and there s-edit and w-edit outputs are all shown in above Figure: 7 and 8. There area and power output are shown below in Figure: 18(a), (b).



(a)

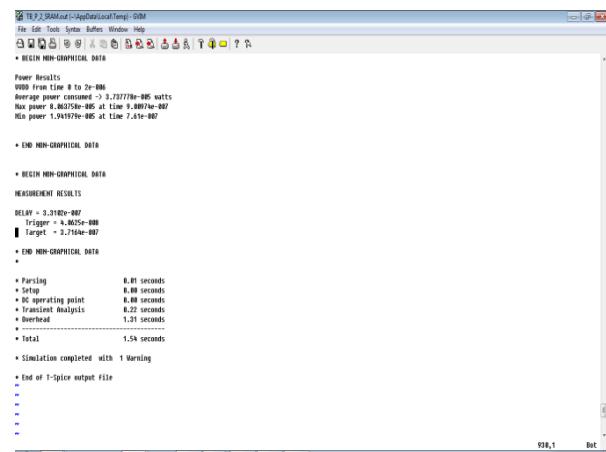


Figure 18. 10T-P2 SRAM area and power output (a), (b)

The 10T-P3 SRAM circuit, Figure: 3(b) and there s-edit and w-edit outputs are all shown in above Figure: 9 and 10. There area and power output are shown below in Figure: 19(a), (b).

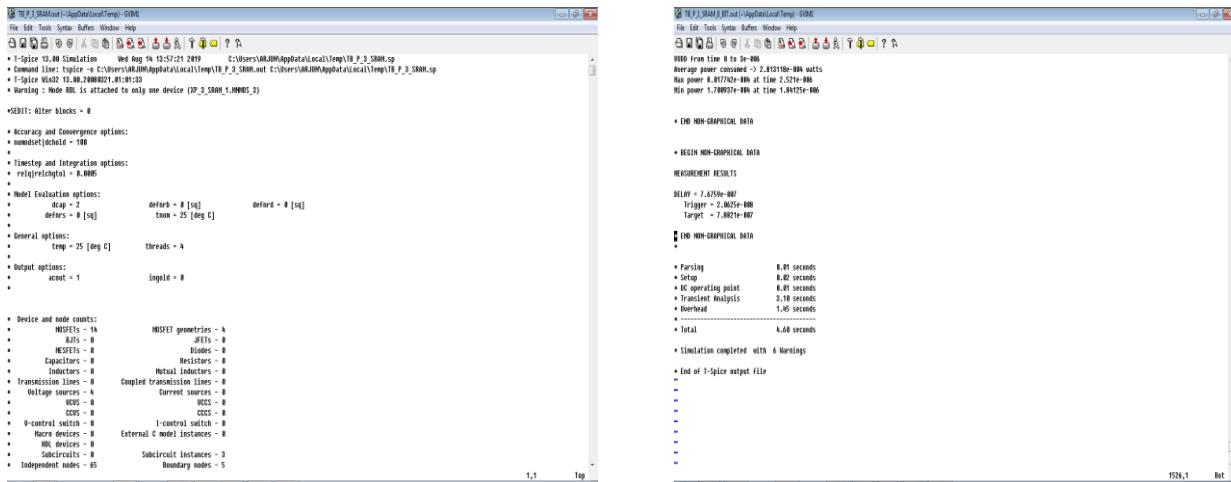


Figure 20. 10T-P1 SRAM using 8 bit area and power output (a),
 (b)

The 10T-P2 SRAM circuit using 8 bit, Figure: 3(c) and there s-edit and w-edit outputs are all shown in above Figure: 13 and 14. There area and power output are shown below in Figure: 21(a), (b).

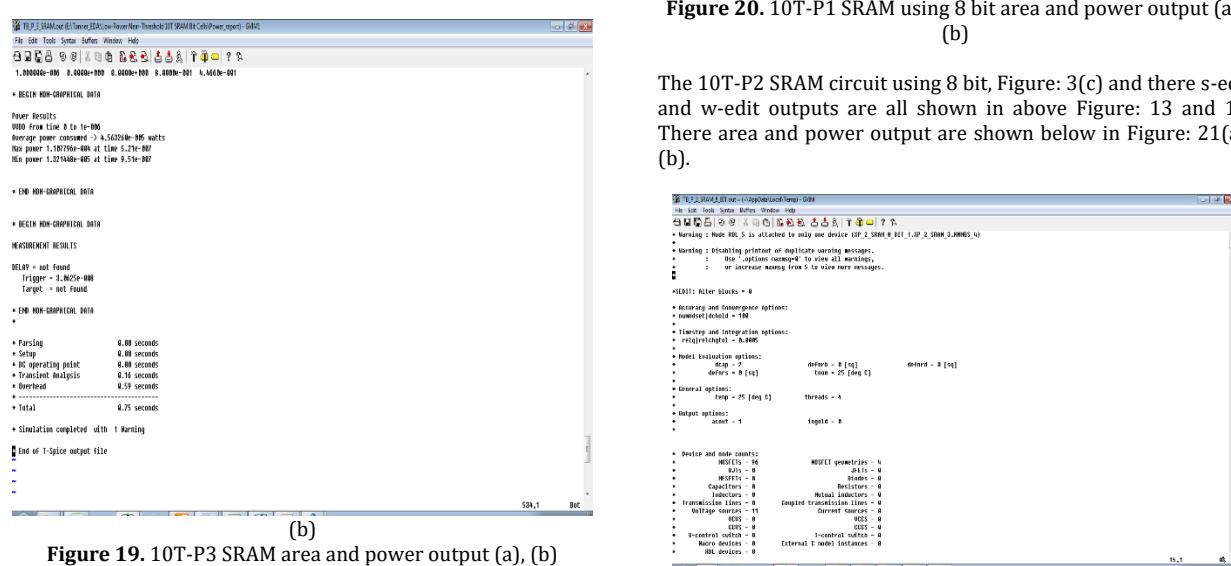
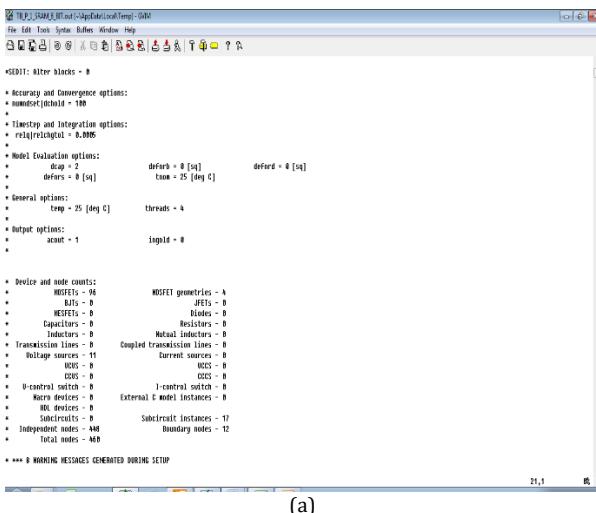


Figure 19. 10T-P3 SRAM area and power output (a), (b)

Area and power outputs for 10T SRAM using 8 bit

The 10T-P1 SRAM circuit using 8 bit, Figure: 3(a) and there s-edit and w-edit outputs are all shown in overhead Figure: 11 and 12. There area and power output are shown below in Figure: 20(a), (b).



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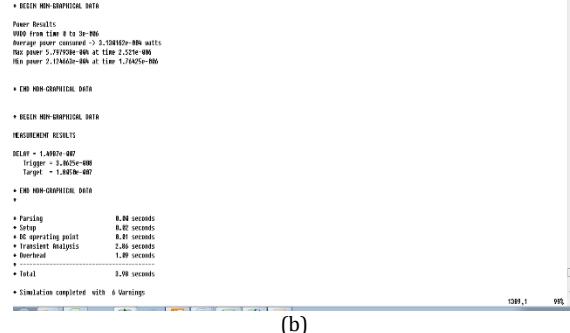
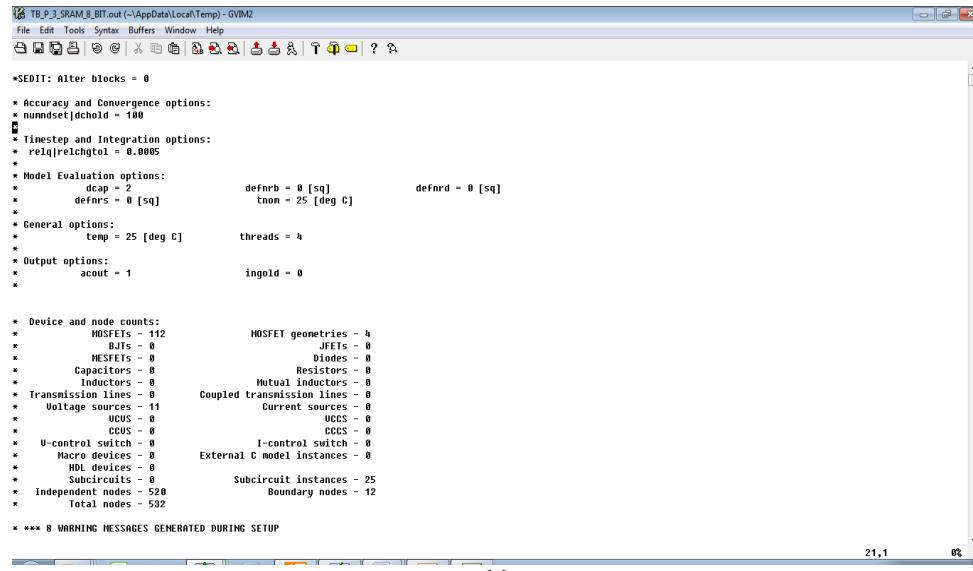


Figure 21. 10T-P2 SRAM using 8 bit area and power output (a),
 (b)

The 10T-P3 SRAM circuit using 8 bit, Figure: 3(b) and there s-edit and w-edit outputs are all shown in above Figure: 15 and 16. There area and power output are shown below in Figure: 22(a), (b).

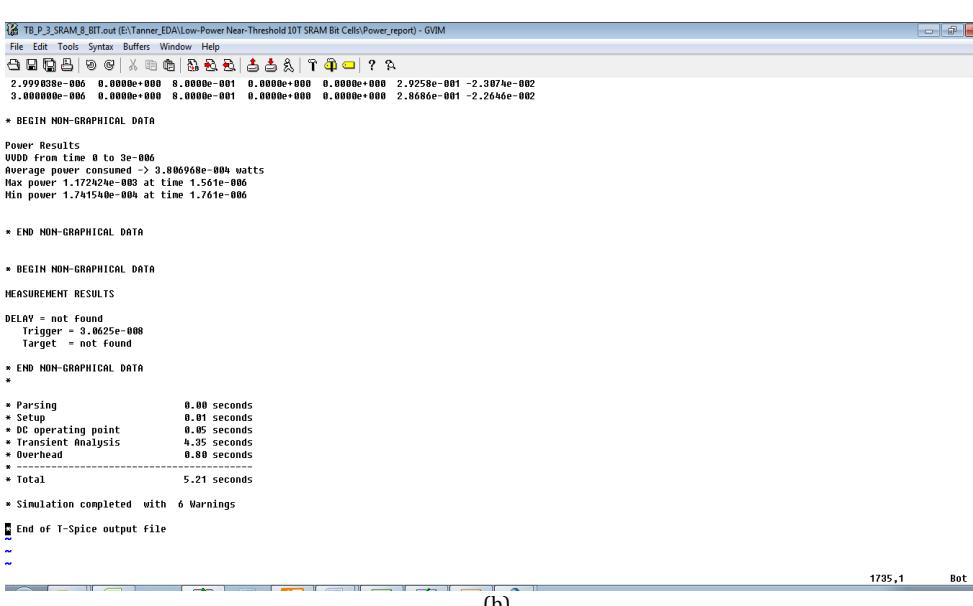


(a)

```

TB_P3_SRAM_8_BIT.out (~\AppData\Local\Temp) - GVIM
File Edit Tools Syntax Buffers Window Help
* SEDIT: Alter blocks = 0
* Accuracy and Convergence options:
* numndstolchold = 100
* Timestep and Integration options:
* relq|relchgtol = 0.0005
* Model Evaluation options:
* dcap = 2 defnrb = 0 [sq] defnd = 0 [sq]
* defns = 0 [sq] tmon = 25 [deg C]
* General options:
* temp = 25 [deg C] threads = 4
* Output options:
* acout = 1 ingold = 0
*
* Device and node counts:
* MOSFETs = 112 JFETs = 0
* BJTs = 0 Diodes = 0
* MESFETs = 0 Resistors = 0
* Capacitors = 0 Mutual Inductors = 0
* Inductors = 0
* Transmission lines = 0 Coupled transmission lines = 0
* Voltage sources = 11 Current sources = 0
* UCVS = 0 UCSS = 0
* CCVS = 0 CCCS = 0
* V-control switch = 0 I-control switch = 0
* Model instances = 0 External C model Instances = 0
* HDL devices = 0
* Subcircuits = 0 Subcircuit Instances = 25
* Independent nodes = 520 Boundary nodes = 12
* Total nodes = 532
* *** 8 WARNING MESSAGES GENERATED DURING SETUP

```



(b)

```

TB_P3_SRAM_8_BIT.out (E:\Tanner_EDA\Low-Power Near-Threshold 10T SRAM Bit Cell\Power_report) - GVIM
File Edit Tools Syntax Buffers Window Help
* BEGIN NON-GRAFICAL DATA
Power Results
WDD Frequency 0 to 3e-006
Average power consumed > 3.005968e-006 watts
Max power 1.72924e-003 at time 1.561e-006
Min power 1.741540e-004 at time 1.761e-006

* END NON-GRAFICAL DATA

* BEGIN NON-GRAFICAL DATA
MEASUREMENT RESULTS
DELAY = not Found
Trigger = 3.0625e-008
Target = not Found

* END NON-GRAFICAL DATA
*
* Parsing          0.00 seconds
* Setup           0.01 seconds
* DC operating point 0.05 seconds
* Transient Analysis 4.35 seconds
* Overhead        0.80 seconds
* -----
* Total           5.21 seconds
* Simulation completed with 6 Warnings
* End of T-Spice output file

```

Figure 22. 10T-P3 SRAM using 8 bit area and power output (a), (b).

Performance Comparison**Table 1.** Comparison between various bits in 10T-SRAM

comparisons	Low-Power and Leakage Reduction in 10T SRAM using Tanner EDA											
	10T SRAM For 1-BIT						10T SRAM For 8-BIT					
	32nm(cmos)			22nm (nmos)			32nm (cmos)		22nm(nmos)			
	10T-P1	10T-P2	10T-P3	10T-P1	10T-P2	10T-P3	10T-P1	10T-P2	10T-P3	10T-P1		
MOSFET	12	12	14	12	12	14	96	96	112	96	96	112
Area(mm)	0.38	0.38	0.44	0.38	0.38	0.44	2.12	2.12	2.46	2.12	2.12	2.46
Delay(us)	30.6	40.6	31.5	30.6	40.6	30.6	20.6	30.6	30.6	20.6	30.6	30.6
Power(uW)	57.6	50.9	1.23	0.33	0.37	0.45	3.26	3.79	5.73	0.02	0.03	0.03

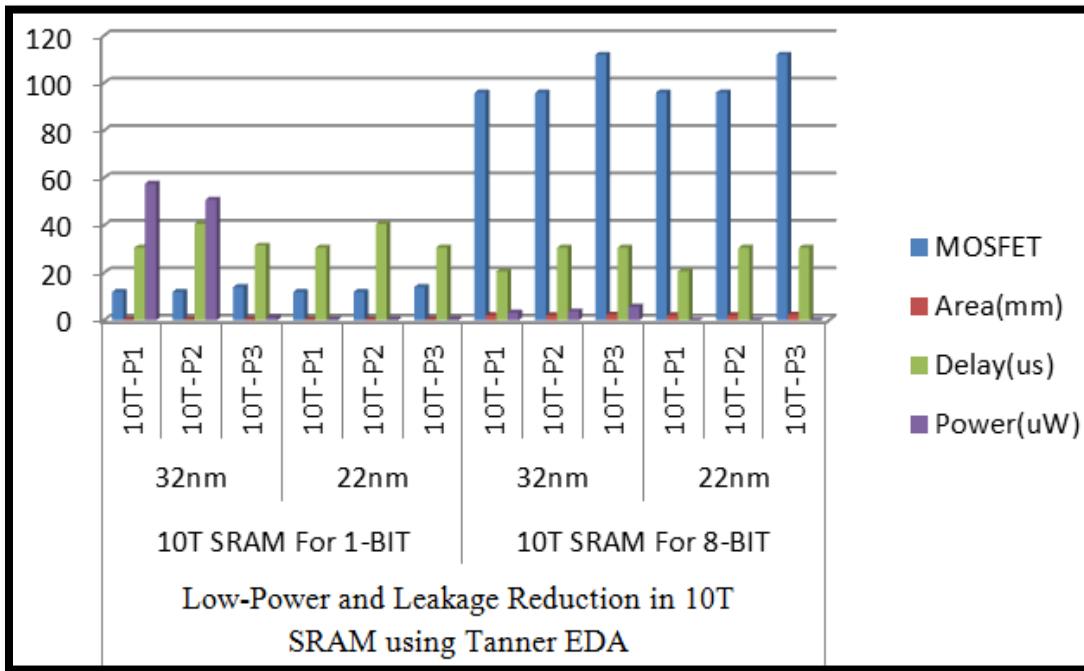


Figure 23. Comparison graph between various bits in 10T-SRAM

CONCLUSION

In above work, we proposed three specific functions on read ports such as low power consumption, space reduction and high performance by data independent read port leakage in SRAM cells. In all the three iteration of read port we used only Nmos to reduce the leakage in SRAM instead of using some Pmos. It also reduced the energy per access and area per cells. The proposed SRAM cells read port shows the effective voltage swing in read bit line, distribution of peripheral circuitry used to save area in the circuit and enable the 1k cell per every read bit. Because of using this unique topology of 10T-SRAM with 22nm technology using tanner EDA software reduces the power utilization up to 80mV in SRAM which led to reduce power consumption and we saved energy per entree up to 30.8% and also saved the area up to 29.5% and observed.

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AUTHORS



R. JEGADEESWARI is pursuing Master of Technology in the stream of VLSI and Embedded System in the Department of Electronics and Communication Engineering, Sri Manakula Vinayagar Engineering College. She received Bachelor of Technology from Sri Manakula Vinayagar Engineering College.



Ramya Jothikumar received Bachelor of Engineering in Electronics and Communication Engineering (ECE) in 2000 and Master of Engineering in Communication systems in 2004 from Madras University and Anna University, India respectively. She completed her Ph.D. program in the Department of ECE, Pondicherry Engineering College. She is currently working as an Associate Professor in the Department of ECE at Sri Manakula Vinayagar Engineering College, Puducherry, India. Her research welfares include wireless communication, MIMO and Digital Communication.



M. MUKILA is pursuing Master of Technology in the stream of ECE and Embedded System in the Department of Electronics and Communication Engineering, Sri Manakula Vinayagar Engineering College. She received Bachelor of Technology from Perunthalaivar Kamarajar Institute of Engineering and Technology.