JOURNAL OF CRITICAL REVIEWS

ISSN- 2394-5125 VOL 7, ISSUE 08, 2020

ANALYTICAL STUDY AND OPTIMIZATION OF LOWER POWER DIGITAL VLSI USING HIGH SPEED SRAM

[1]Divya Kanuganti, [2] Dr.Anil Kumar

[1]Sri Satya Sai university of Technology & Medical Science, Email: divyakanuganti.ece@gmail.com

[2] Sri Satya Sai university of Technology & Medical Science

Abstract

The general performance of the method is actually dominated the majority of the time, by the SRAM which makes up a big portion of a system-on-chip region. Furthermore, the fast growth as well as the acceptance of mobile, hand held equipment along with other emerging programs, like WSNs (wireless body sensing networks) implanted medical instruments, necessitates the necessity of low power SRAMs. Hence, there exist necessities of a strong low power SRAM circuit style and is now crucial. Nevertheless, a look of robust low power SRAM faces many progressions as well as performance connected obstacles.

1.1 introduction

Growing need for handheld devices such as for instance cellular phones has motivated the semiconductor market into a novel low energy as well as low power frontier. In order to boost the battery life phase for as comprehensive as they can, a limited amount of energy kept in undersized battery must have large power management methods. Once again, capability of the electric battery has been created at the modest speed (two to 3 times during the last thirty years). Embedded SRAM occupies greater than sixty-five % of the video decoder's center region of a chip and contributes to in excess of thirty % of mobile device power consumption.

With technological development top demanding for items that are brand new as well as designs with brief style time as well as price components, a lot of the models which were utilized in developing two complicated VLSI circuits haven't been in a position to adopt innovative and simple methods to bring down power. Moment to promote being shorter, a lot of engineers haven't attempted or even have failed to deal with several of the smart methods which could be followed to greatly reduce power at circuit amount, sub system level as well as at the architecture amount. To be able to minimize power, it's necessary to recognize the functional and architectural needs before choice of appropriate reduction methods.

With all the growing need of portable digital methods, VLSI business a lot focusing on the low power consuming products. This's due to the demand of portable device is elevated tremendously. It's hard for charging portable unit often. They need to be built with huge capacity batteries to be able to stay away from regular charging. Huge battery packs carrying on device that is portable is tough also and again costly.

1.1.1 VLSI – DIGITAL SYSTEM

Very Large-Scale Integration (VLSI) is actually described as a single chip integrated circuit consists of transistors and it's a one-time silicon chip that contains the collections of gates fabricated. Inside VLSI chips, the power consumption has grown continuously. Moore's law says that VLSI technique is utilized to increases in clock frequencies as well as transistor density continually. The VLSI development know-how scaling in the couple of years show that40 % increase in number of on chip of transistors as well as thirty % increases in frequency operation of VLSI methods. The supply voltage as well as capacitance scale down the VLSI chips power consumptions and it's increasing constantly. For the high-performance VLSI chip layout, back end as well as front end methodology has a crucial effect on the layout time, style power, style speed, style delay as well as style cost.

1.1.2 VLSI Design Flow

The VLSI IC circuit's configuration flow is appeared in the figure below. The different degrees of configuration are numbered and the squares show measures in the plan flow. Particulars starts things out, they portray uniquely, the usefulness, interface, and the engineering of the computerized IC circuit to be planned.

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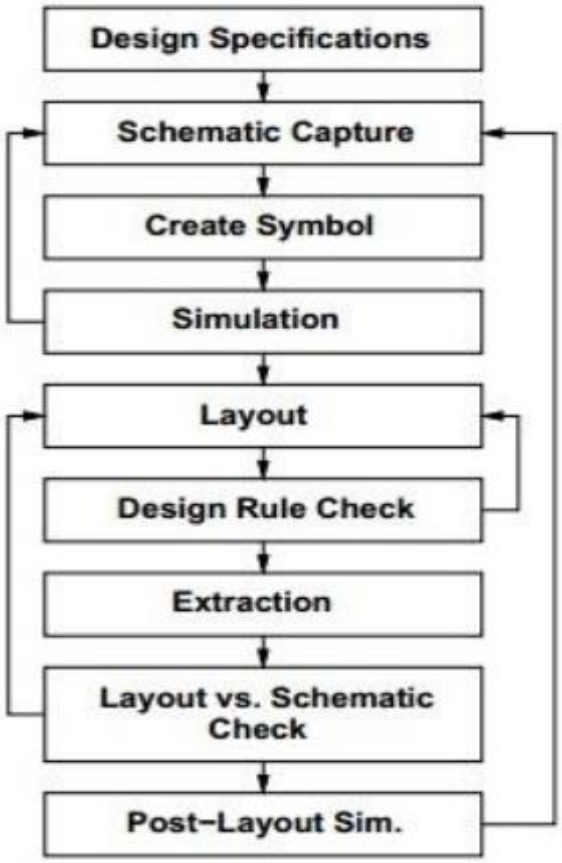

Figure 1: Simplified VLSI Design Flow

RTL depiction is then changed over to a gate-level net list utilizing rationale blend instruments. A gate level net list is a portrayal of the circuit as far as gates and associations between them, which are made so that they meet the circumstance, power and zone particulars. At last, an actual format is made, which will be confirmed and afterward shipped off manufacture.

1.1.3 OPTIMIZATION TECHNIQUES

The principal optimization technique was proposed by Cauchy in the year 1847 for taking care of unconstrained nonlinear optimization issues. This technique is known as steepest plummet strategy. Nonetheless, the idea of optimization was accounted for in before. In 300 B.c., Euclid initially thought about the insignificant separation between a point and a line. He additionally demonstrated that a square has the best region among the square shapes with the given edge. In 200 B.c., Zenodorus tackled another optimization issue known as Dido's concern: "Discover the figure limited by a line which has the greatest region for a given edge". The arrangement of this issue is half circle. In 100 B.c., Heron demonstrated that light goes between two focuses through the way with briefest length while reflecting from a mirror. In the seventeenth, eighteenth and first 50% of nineteenth century, a few scientists created/proposed various speculations/properties identifying with optimization. Among these, the innovations of math of varieties, secretary issue, assemblage of insignificant obstruction, rule of least activity, least square technique, idea of inward capacity, transportation issue, direct programming issue and so on merit referencing.

1.2 LITERATURE REVIEW

Pal, Antardipan& Zhang (2020) There is an incredibly popularity for a rapid, low power, low spillage, and low clamor Static Random-Access Memory (SRAM) for superior store recollections. The energy effectiveness of SRAM is of principal significance in both elite and ultralow-power convenient, battery worked electronic frameworks. In this article the components influencing the general speed and complete energy utilization of a traditional 6T SRAM cell/cluster with 6 FETs, especially functions of access transistors are examined to feature the necessities and headings for development. A crossover 6T SRAM with two access FETs being supplanted by light-effect transistors (LETs) and the electrical word lines supplanted by optical waveguides (OWGs) is proposed. This half breed SRAM is broke down to uncover its potential in improvement of the exchanging velocity and consequently complete energy consumption over the ordinary 6T SRAM. Mathematical examinations of a model mixture SRAM exhibit of 64 KB show a factor of 7 and 34 decrease in read deferral and read energy utilization, individually; and 4 and 6 in compose postpone and compose energy consumption, separately, when the access FETs are supplanted by

LETs. The likely effects on the fringe and help circuits because of this crossover structure and utilization of the LETs there are likewise quickly examined.

G Poornima (2019) every year chip center is shrivelling attributable to the progression in innovation and diminishing in innovation hub. The new difficulties incorporate more tough and thorough execution targets contrasted with past venture. Execution targets incorporate planning, power just as territory optimization. With every new plan of microchip center there can be a prerequisite of new methods to be added to the current once. The primary objective is to improve Timing just as Power to accomplish higher calibre of plan through cell resizing, rationale optimization, clock tuning, CTS, double/quad inclusion. Working recurrence and voltage are fixed for each undertaking. Action Factor is a steady amount contingent upon the plan. The optimization strategies referenced in this work, centers around decrease of dynamic capacitance and the protection from diminish the dynamic power of the circuit. These strategies referenced in this paper are tried and results dissected.

Mehra, Krishan & Sharma (2019) in the semiconductor business, while planning advanced framework memory segment assumes a critical function on chip. For quite a while now, we have been dealing with the memory planning yet the cycle needs adjustments every year. At first we are chipping away at planning of CMOS based SRAM, following which we took a shot at multi gate semiconductor, for example, plan of FinFET based SRAM. As of now we are taking a shot at the last mentioned, in light of the fact that with the ascent in number of semiconductors, the on-chip locale likewise expands, which is the reason we are chipping away at diminishing the chip region just as the power utilization nowadays. With the innovation scaling the size of the semiconductor is diminished however this will influence unsteadiness of SRAM cell. As the innovation scaling is done the SRAM cell is worked below edge locale. The significant worry with working SRAM below edge locale is the cycle variety impacts which will cause to semiconductor jumble and furthermore corrupt the static commotion edge.

Surwadkar, Tushar &Purkayastha (2019) FinFETs have been utilized in an assortment of imaginative manners in computerized and simple circuit plans. The two entryways for FinFETs give successful control of the short-channel impacts without forcefully downsizing the door oxide thickness and expanding the channel doping thickness. The different biasing in DG gadget effectively gives various limit voltages. It can likewise be misused to diminish the quantity of semiconductors for actualizing rationale capacities. The objective of this examination work is likewise to investigate FinFET rationale configuration styles like SG, IG, LP, and IG/LP and study their suggestions for low-power plan and additionally locate the best mode as far as power utilization. It was assessed that spillage power may represent as much as half of the of the absolute power utilization in CMOS circuits. Spillage power utilization was seen to stay around more measure of the complete power on a normal we investigate strategies to effectively conquer this test through a blend of circuit plan methods and rationale level optimization. It considers the utilization of IDDG-FETs in advanced CMOS configuration, zeroing in on the utilization of free door FinFET. Record Terms-FinFET, HSpice Simulation, NAND door and Power dissemination

Alberto Wiltgen (2013) Memory is the significant piece of the greater part of the electronic frameworks however the serious issue with the plan of recollections is execution of gadgets for example speed and power scattering. In this paper execution for read, compose activities of SRAM cells dependent on various setups are thought about, explicitly in every cell plan the static-noise-margin (SNM) is determined by noticing butterfly trademark bends. As indicated by the outcome investigation the 7T SRAM cell in 45nm CMOS innovation has less power dispersal and power postpone item since it utilizes single bit for both peruse and compose activities. The complete hardware is planned and re-enacted by utilizing Cadence virtuoso and phantom individually.

Alioto, M, Di Cataldo, G & Palumbo (2007) In view of the framework varieties of little utilitarian size, improved change capacities in pieces are getting increasingly imperative, as innovation hubs continue to scale, essential memory experience expanded energy with yield and time effects, for example, crosstalk, challenges in utilization and dependability. We recommend a maintainable system to blunder amendment in profoundly scale recollections to handle expanding disappointment rates attributable to issues. SRAM is often utilized for rapid memory applications like reserve.

L.Saranya (2018) In past, the size of electronic gadgets were large, required more power, disseminated more measure of warmth and hence it was not dependable. Thus, there was a need to lessen the size of these gadgets and their warmth dissemination. This brought forth the creation of innovation which is called as VLSI innovation. The power optimization is the significant test in the VLSI advances; SRAM is generally utilized part in on chip recollections, convenient supplies, rapid processors, and CPU reserve memory and hard drive cushions.

Saranya, L & Chakrapani, Arvind (2018) the approach of compact gadgets in our everyday life nas made Power Optimization as one of the significant difficulties in the advanced VLSI innovations. Static Random access memory (SRAM) has been broadly utilized in the on-going days because of its superior in VLSI plan procedures which works in the scope of submicron or Nano range. In the SRAM cell, the scaling of

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semiconductor will expand the security of the cell at the hour of peruses and composes activity. There are a few SRAM cells has been planned which works at the lower voltage with less postponement. SRAM is favoured because of its basic development, low power necessities, low access time, speed and unwavering quality when contrasted with Dynamic Random Access Memory (DRAM). SRAM is utilized as primary memory for little reserve less implanted processors. Thus development of recollections utilizing SRAM cell which is upgraded as far as cycle boundaries in particular power, thickness, territory and deferral is an expected region for research and the equivalent is introduced in this article.

Bodapati, Dr & Sharma (2017) Presently a day there has been extending interest for quick progressed circuits at low power use. The extending criticalness of low power usage is required to routinely reducing the component size of microelectronic circuits. Low power gadget arrangement is at present a basic field of Research due to increase the solicitation of helpful gadgets .In this paper a methodology is presented. For restricting the power usage for cutting edge system This paper gives a blueprint of restricting the power usage in a mechanized accumulating components, like Flip Flops, Latches and so forth Flip Flops are key amassing components in cutting edge circuits .In this paper a couple of strategies is discussed for low power use in a limit part. The Techniques are as, GDI (Gate scattering input) Technique and Modified GDI Technique. The low power methods that are acquainted have been associated with layout of low power progressed limit components. Two kinds of domino rationale circuits to be explicit I) 16 digit domino rationale multiplexer and ii) 4bit 4 yield domino rationale pass on generator are considered as test circuits. Three other spillage decline methodologies specifically Standard Single (low) limits voltage (Single-Vt), twofold edge voltage (twofold Vt) and Variable Body Biased Keeper (VBBK) are similarly associated with these circuits and explored. The results exhibit that by virtue of multiplexer; the proposed AVL multiplexer gives the lowest spillage.

Syed, Munaf& Lakshmanan (2017) Recollections are the urgent piece of any computerized framework and no advanced framework can be finished without recollections. Conservative gadgets and installed frameworks are arising, so the low power utilization is very basic to the structural framework plan .Optimization of the power at the intelligent level is one of the main undertaking to limit the power. With expanding innovation, use of SRAM Cells has been expanded in large degree while planning the framework on-contributes CMOS innovation, this survey article is likewise founded on that. In this article centers around the investigation in wording uncommon sorts of SRAM are planned to fulfill low power, elite, postponement and territory.

MortezaNabavi et al. (2016) have proposed an ideal pMOS to nMOS width proportion which prompts the most noteworthy working recurrence in the sub threshold locale. This ideal worth can be acquired by finding the most extreme current over capacitance proportion by limiting the deferral of an inverter logically and mimicking distinctive CMOS entryways in the sub edge locale. Simulation results shows that the recurrence of activity achieves its greatest at the ideal PMOS to NMOS width proportion autonomous of the gracefully voltage.

Liang H et.al (2016) recommended the methodology of BIST needs to conclusion blame and recognizes issue SRAM-based FPGAs. This paper shows FPGA BIST structure, which has CLB and interconnect shortcomings. This deficiency comprises short/open just as defer shortcomings that present in the channel of wire. Different blames to be specific stuck on/off issues in PSs, stuck-at-0/1 blames in LUTs. The XC4000-arrangement deficiencies in the channel has tried and indicated suitable execution in issue inclusion, time required for test, and space accomplished by BIST structure. This structure contrasted and the proposed FPGA BIST structure achieves the capacity for analyse of deficiencies on CLBs.

Methodology

1.3 LOW POWER MEMORY DESIGN

Because of the rise in multimedia data transmission, memory requirements of today's embedded systems have skyrocketed. This situation is largely due to advancements in 5G and 6G technologies. The VLSI industry is extending the amount of memory usable in electronic media to meet the demands of 4G and 5G technologies (Bushnell et al., 2004). As a result, memories eat up more than half of the die surface area. Embedded devices use a lot of resources as a result of this. Increased heat dissipation is caused by high power consumption in VLSI circuits. Additional heat sinks are needed to minimize heat dissipated due to high power consumption. In addition, special manufacturing methods must be modified, resulting in an improvement in device costs.

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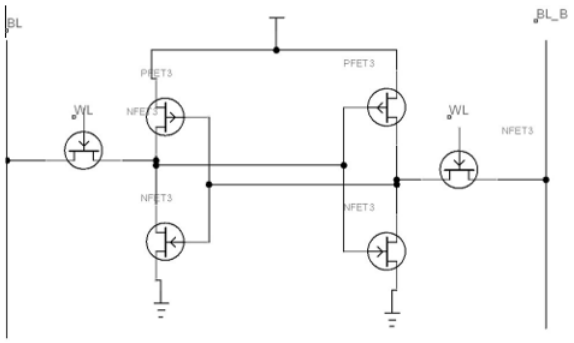

Figure 2 SRAM 6T Cell

Random-Access Static The key memory block of cache memories is memory. The circuit diagram of a regular SRAM 6T cell is shown in Figure 1. The power output gain in any embedded circuit is highly affected by the low power SRAM construction (Yamaoka et al., 2004). According to Moore's projections, the decrease in supply voltage due to technical scaling has a major influence on power demand year after year. However, scaling causes a large rise in static leakage current (Nii et al., 1998). There are some other parameters that change the device behavior as the technology scales beyond 10nm. As a result, design engineers are searching for cost-effective approaches to technology scaling for low-power device architecture.

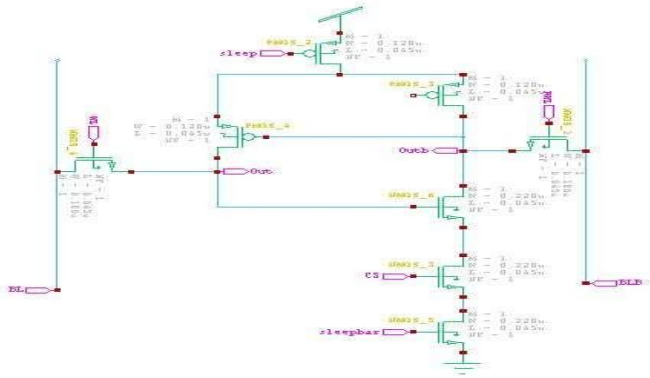

Figure 3 Modified MTCMOS with sleep transistorarchitecture

1.4 PROPOSED Methodology

During the idle period, leakage current can be used to measure static power. In idle mode, the access transistors are turned off, and the bit lines are charged to VDD. The proposed SRAM configuration is narrow and has a wide VDS (Voltage Drain Storage). In standby mode, WL, WR, and RD are all set to 0V logic nil. A sleep transistor is present in the proposed design while it is in idle phase, which helps to reduce leakage capacity. To minimize leakage power, the proposed design uses transistors with several threshold voltages. As compared to higher threshold voltage circuits, lower threshold voltage (Vth) systems will save approximately 30% on power consumption.

$$P_s = V_{dd} * I_{Leakage} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots 1$$

And the complex force can be stated as follows:

$$P_d = \alpha C_1 V_{dd}^2 f \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots 2$$

The updated MTC-MOS Static Random-Access Memory architecture is seen in Figure 2. The transistors used to apply logic have all been designed with a low threshold voltage. Low threshold voltage transistors are used in this logic. Pull-up and pull-down logic blocks are implemented using low threshold voltage transistors. The 8X8 SRAM schematic is seen in Figure 3 using a modified MTCMOS architecture.

Table 1 displays the cumulative and static power usage of various SRAM systems based on simulation data. Normal SRAM, Memristor-based SRAM, MTCMOS-based Memristor SRAM, and the planned SRAM design are all examples of SRAM technology are all compared. The proposed SRAM structure has a significant reduction in total and static control, according to comparative data. Figure 4 depicts a schematic

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description of the effects of static and total power usage comparisons with various SRAM structures. These findings were obtained at room temperature for various SRAM structures. Table 2 compares the effects of different SRAM structures' power usage at various temperatures. Figure 5 depicts the graphical depiction of different SRAM structures' power consumption at various temperatures. The power consumption of various SRAM structures does not improve much at low temperatures, but it does decrease significantly at high temperatures, according to the experimental findings.

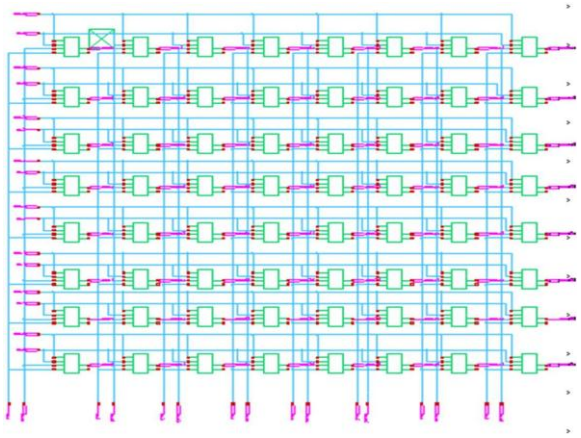
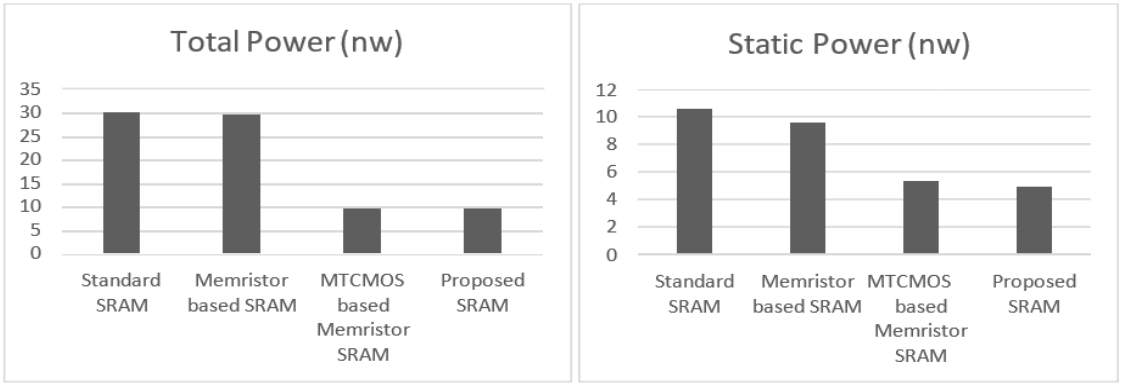


Figure-4. 8X8 SRAM schematic with implemented SRAM architecture



(a) (b)

Figure 5 Complete and static power for various SRAM architectures was contrasted.

Table 1 For various SRAM architectures, cumulative power and static power are measured.

SRAM	Voltage (v)	Total power (nw)	Static Power (nw)
Standard SRAM	0.7	30.90	10.59
Memristor based SRAM (Baghel et al., 2015)	0.7	29.69	09.61
MTCMOS based Memristor SRAM	0.7	09.84	05.30
Proposed SRAM	0.7	08.28	04.89

Table 2 At different temperatures, the total strength of different SRAM cells

SRAM	Temp 10ºC nw	Temp 25ºC nw	Temp 40ºC nw	Temp 55ºC Nw
Standard	06.79	06.90	30.90	48.10

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SRAM				
MTCMOS SRAM	04.90	06.43	09.84	18.12
Proposed SRAM	03.05	03.47	08.28	12.08

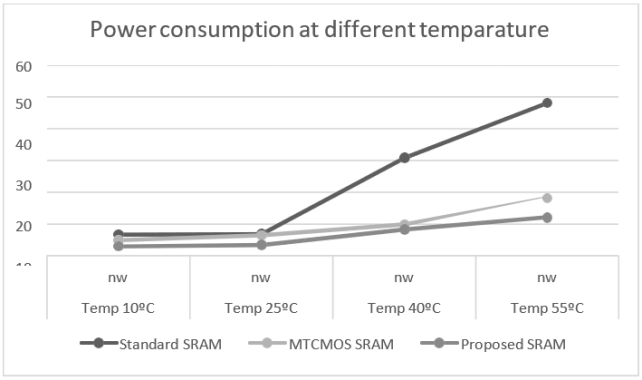

Figure 6 A graph depicting the power usage of various SRAM systems.

A new architecture for SRAM construction is presented in this article. Memory power use is divided into two categories. One part is static power, and the other is dynamic power. Static power is given by leakage current while the SRAM is idle, whereas dynamic power is generated by the switching of either cell from 0 to 1 or 1 to 0. Because of the short lengths and widths of the transistors as the process scales above 75nm, leakage current plays a major role in total power consumption. To mitigate leakage current, the proposed strategy is to construct a revamped MTCMOS architecture. The proposed design is tested at various temperatures and compared to a conventional 6T SRAM system. As compared to standard architecture at rated temperature, experimental findings indicate an approximately 21% reduction in power consumption in the proposed 8X8 SRAM architecture.

1.5 Data Analysis and Results

The challenges are growing in tandem with the advancement of creativity. We will extend our test if we go to convey capacity. The topic of warming begins in battery-operated units. In this way, we can verify the memory ability of every electronic system before purchasing it. We question about the volume of RAM in the electronic system. Everyone in the portable unit needs unrestricted access.

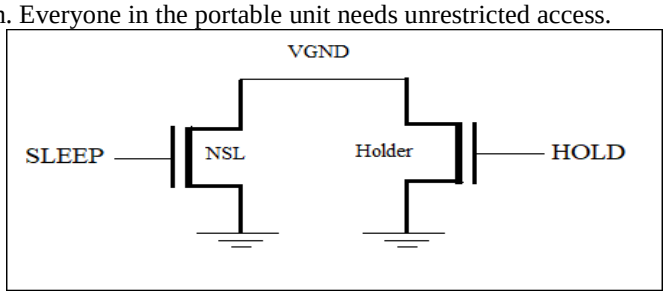

Fig 7: Techniques of 6TSRAM Ground-Gated

1.6 Results on 6T SRAM Cell

Excursion stage at 180nm innovation: The 6T SRAM circuit has two output ports. All outputs are complementary to one another. The first output socket, 'Q,' is set to Vdd, while the second, 'Q bar,' is set to '0' volts. Find the excursion point using Table 4.1 and a number of noise source voltages.

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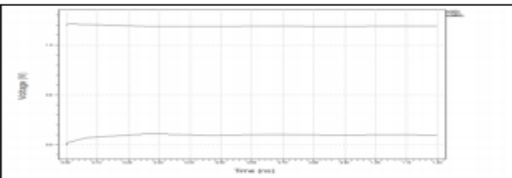
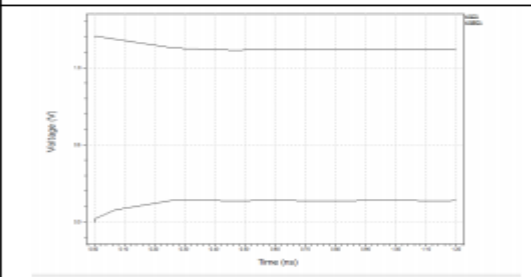
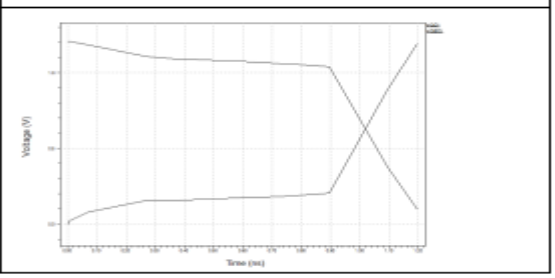
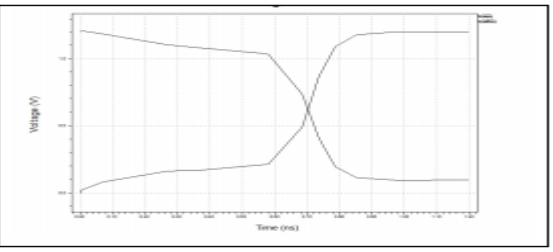
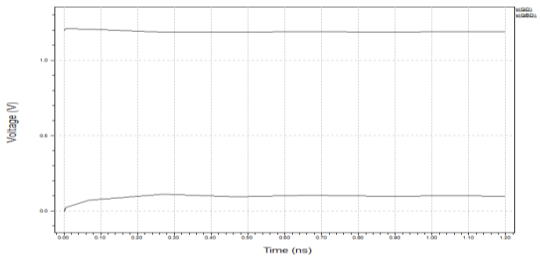
Table 3: Noise Voltage Source Output state

S.No.	Noise Source	Simulation Result (initially: Q=V_{dd} and Q_bar=0) Scale:- X-Axis: Time(ns);Y-Axis: Voltage(volts)
1.	.25volt	
	.32 volt	
	.335 volt	
	.34 volt	

4.2 Result on Conventional 6T SRAM cell

The point of exit is creativity. 65nm: This experiment is completed using the 65nm technology described in Table 4.3.

Table 4 Noise Voltage output states Source on 70 nm

S.No.	Noise Basis	experimental Result (initially: Q=Vdd and Q_bar=0) Scale: - X-Axis: Time(ns);Y-Axis: Voltage(volts)
1.	.25volt	

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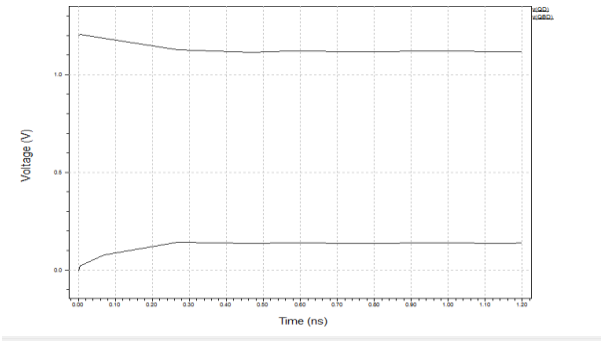
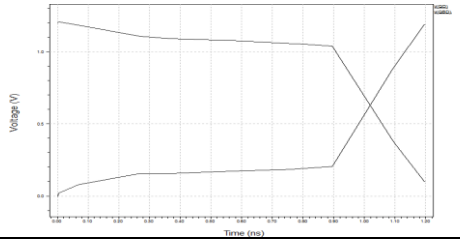
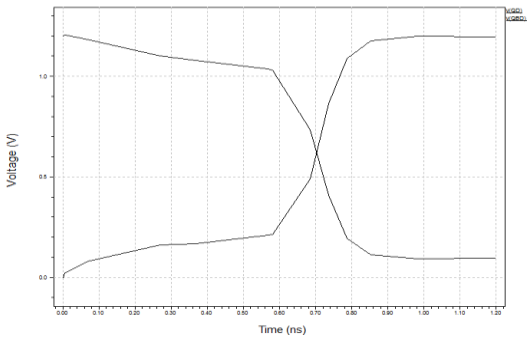
2.	.32 volt	
3.	.335 volt	
4.	.34 volt	

Table 5: States of Power Supply Versus Flipped

Voltage	Noise Source Voltage
1V	0.16
1.5V	0.21
2v	0.31
2.5V	0.36
3V	0.41
3.5v	0.43
4v	0.45
4.5v	0.45
5v	0.43

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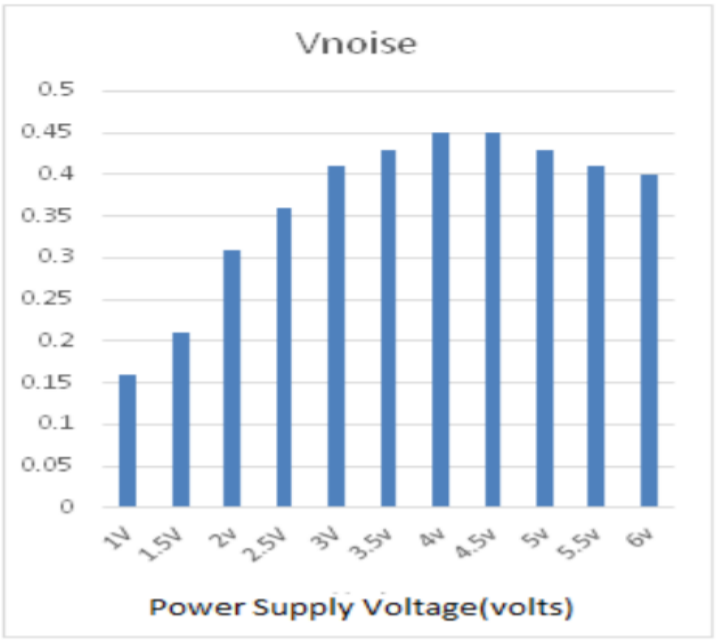
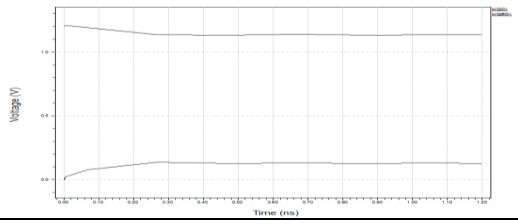
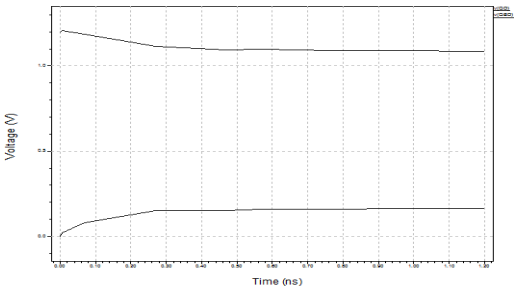


Fig : Power Source Conditions Versus Flipped

Table 6: Active Mode Noise Voltage output state Source

S.No.	Noise Source	experimental Result (initially: Q=Vdd and Q_bar=0) Scale: - X-Axis: Time(ns);Y-Axis: Voltage(volts)
1	.31 volt	
2	.33 volt	

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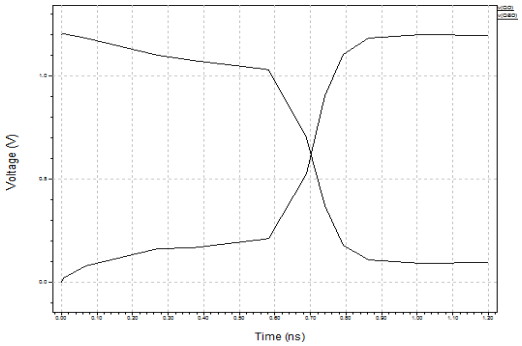
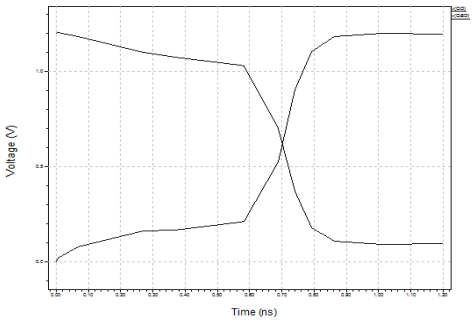
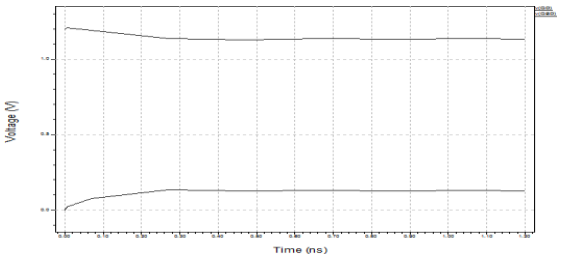
3	.34 volt	
4	.35 volt	

Table 7: Sleep Mode Noise Voltage output state Source

S.No.	Noise Basis	experimental Result (initially: Q=Vdd and Q_bar=0) Scale: - X-Axis: Time(ns); Y-Axis: Voltage(volts)
1.	.31 volt	

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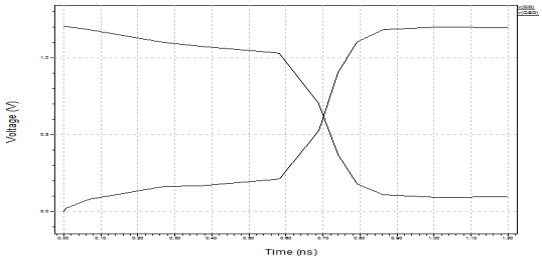
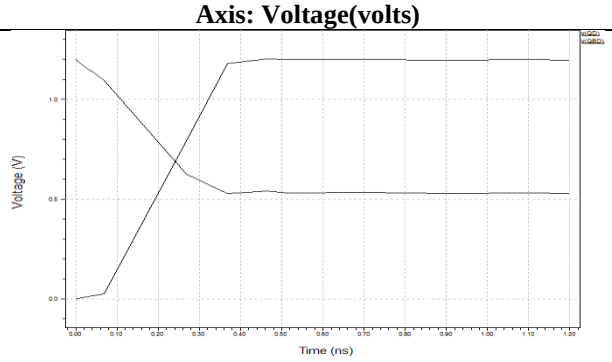
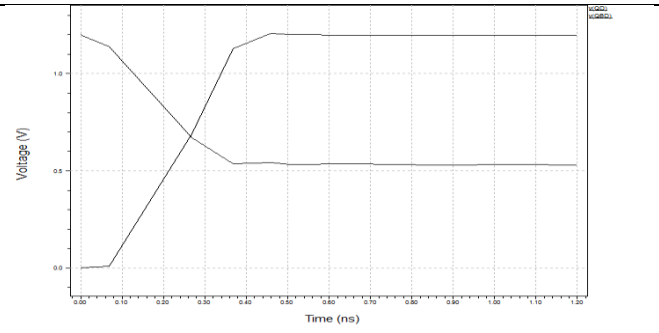
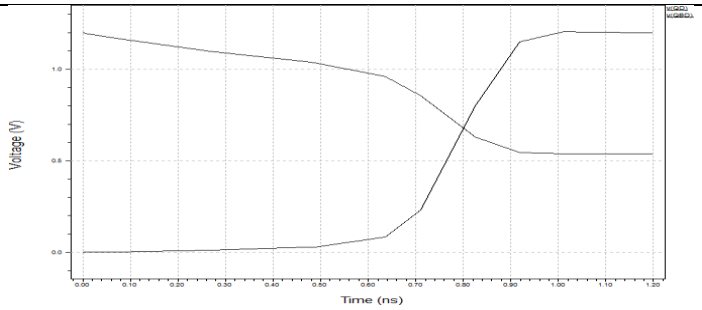
2.	.34 volt	

Table 8 Noise Voltage output state input of 8T SRAM Asymmetrical cell

S. No.	Noise Source	experimental Result (initially: Q=Vdd and Q_bar=0) Scale: - X-Axis: Time(ns);Y-Axis: Voltage(volts)
1.	0.46 volt	
2.	.43 volt	
3.	.39 volt	

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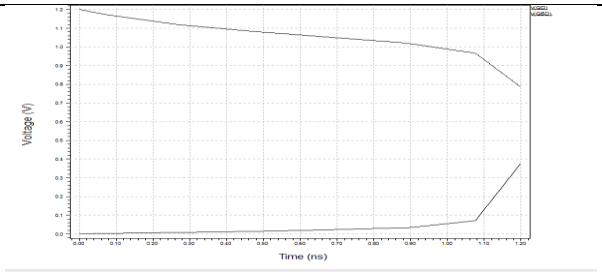
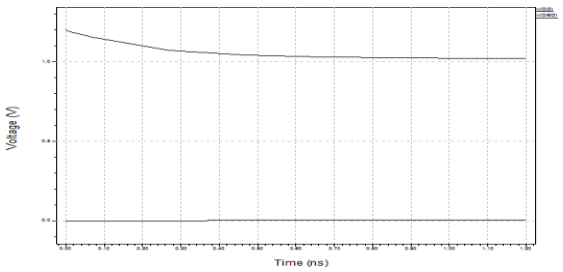
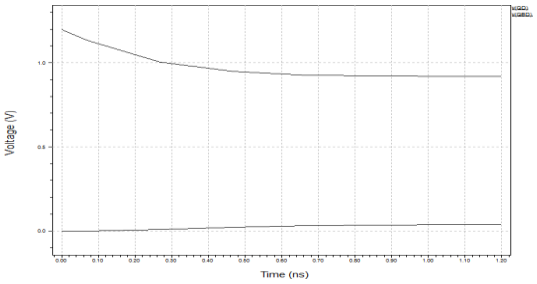
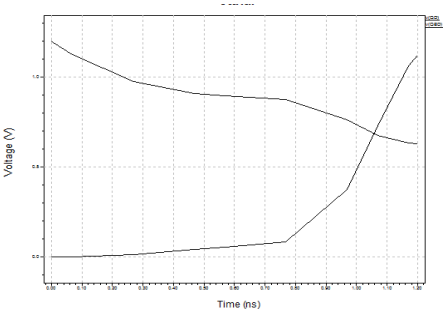
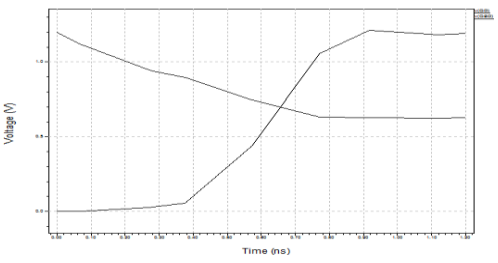
4.	.38 volt	

Table 9: Noise Voltage output state input of 9T SRAM Asymmetrical cell

S.No.	Noise Source	experimental Result (initially: Q=Vdd and Q_bar=0) Scale:- X-Axis: Time(ns);Y-Axis: Voltage(volts)
1.	.25 volt	
2.	0.28 volt	
3.	0.29 volt	
4.	0.30 volt	

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Conclusion

Many organizations work in building memories with low power dissipation as well as high efficiency. SRAMs are actually recognized to dissipate high power. They're essential in a number of uses which include System on Chips (SoCs). Thus, interest is paid towards developing energy that is low as well as high efficiency SRAM cells as well as architectures. The adder and also the memory are actually the 2 great building blocks of any digital system. Thus, this particular thesis analyses several SRAM as well as adder cells with a unique focus on variability as well as power dissipation and also proposes circuit amount strategies to reduce both power dissipation and variability.

References

[1.] Pal, Antardipan& Zhang, Yong &Yau, Dennis. (2020). Proposal of a FET-LET Hybrid 6T SRAM.

[2.] G Poornima.(2019). Timing And Power Optimization In Digital VLSI Circuits. The International journal of analytical and experimental modal analysis. Volume XI, Issue VIII, August/2019

[3.] Mehra, Krishan & Sharma, Tripti. (2019). Analysis of SRAM cell design: a better perspective for reducing the chip area and power consumption by increasing the stability of SRAM cell. ICAICR '19: Proceedings of the Third International Conference on Advanced Informatics for Computing Research. 1-7. 10.1145/3339311.3339338.

[4.] Surwadkar, Tushar &Purkayastha, Arnab & Shah, Varsha & Shaikh, Nargis. (2019). IMPROVING PERFORMANCE OF VLSI CIRCUITS USING DIFFERENT MODES OF FINFET. 6. 25.

[5.] Alberto Wiltgen.(2013). Power Consumption Analysis in Static CMOS Gates. 978-1-4799-1132-5/13/$31.00 ©2013 IEEE

[6.] Alioto, M, Di Cataldo, G & Palumbo, G 2007, 'Mixed full adder topologies for high- performance low power arithmetic circuits', Microelectronics Journal, vol. 38, pp. 130-139.

[7.] L.Saranya.(2018). A SURVEY ON LOW POWER COMPARISON IN SRAM CELL. International Journal of Pure and Applied Mathematics. Volume 118 No. 20 2018, 611-616

[8.] Saranya, L & Chakrapani, Arvind. (2018). Survey on the design methods of low power SRAM cell. International Journal of Pure and Applied Mathematics. 118.

[9.] Bodapati, Dr & Sharma, Vidushi&Supervisor,. (2017). AN ANALYTICAL APPROACH OF LOW POWER CONSUMPTION IN DIGITAL SYSTEMS USING CMOS DIGITAL VLSI CIRCUITS. 2320-6144.

[10.] Syed, Munaf& Lakshmanan, Malathi&Dr.A.Bharahi, & A.N., Jayanthi. (2017). Review on Power Dissipation Analysis of Conventional SRAM Cell Architecture. International Journal of Advanced Research in Computer Engineering & Technology (IJARCET). 6. 1764 - 1768.

[11.] Liang, H. ―A Methodology for Characterization of SET Propagation in SRAM-Based FPGAs‖, IEEE Transaction Nuclear Science, Vol. 63, No. 6, pp. 2985–2992, 2016.