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Signal Powered Low Drop Diode Equivalent For Energy Harvesters

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***Abstract*-. Piezoelectric-device-based vibration energy harvesting requires a rectifier for conversion of input ac to usable dc form. Power loss due to diode drop in rectifier is a significant fraction of the already low levels of harvested power. The proposed circuit is a low-drop-diode equivalent, which mimics a diode using linear region-operated MOSFET. The proposed diode equivalent is powered directly from input signal and requires no additional power supply for its control. Power used by the control circuit is kept at a bare minimum to have an overall output power improvement. Diode equivalent was used to replace the four diodes in a full- wave bridge rectifier, which is the basic full-wave rectifier and is apart of the more advanced rectifiers like switch-only and bias-flip rectifiers. Simulation in 130-nm technology and experiment with discrete components show that a bridge rectifier with the proposed diode provides a 30–169% increase in output power extracted from piezoelectric device, as compared to a bridge rectifier with diode- connected MOSFETs. The bridge rectifier with the proposed diode can extract 90% of the maximum available power from an ideal piezoelectric device-bridge rectifier circuit. Setting aside the constraint of power loss, simulations indicate that diode drop as low as 10 mV at 38 μA can be achieved.**

***Index Terms*—Full-wave bridge rectifiers (FBRs), low-drop- diode equivalent (LDDE), piezoelectric devices (PZDs), syn- chronous rectifiers, vibration energy harvesting.**

I. INTRODUCTION

AMBIENT vibration energy can be harvested and converted to useful electrical energy. The electrical energy can be used for powering low-power electronic systems such as sen- sors, microelectromechanical systems devices, or implantable medical electronics. Vibration energy can be harvested using various types of transducers such as electromagnetic, elec- trostatic, or piezoelectric. Electromagnetic-device-based har- vesters employ a coil to tap energy from a moving magnetic field produced by magnets, which move in the ambient vibra- tion [1]. In electrostatic energy transducers, vibration leads to a relative parallel motion between an electret and nearby metallic surface [2]. This leads to induced counter charge on the metal, with the charge simply following the relative motion of the elec- trets. This produces an electric current. Piezoelectric harvesters work by stressing a piezoelectric material in accordance with the vibration and tapping the generated electric charge from the material. Electrical energy from any vibration energy harvester de- vice is converted to a load-usable form by an interface circuit, which is connected between the device and its load. The inter-face circuit consists of a rectifier–filter section for conversion of input ac to dc. The diodes in the rectifier conduct with a volt- age drop, leading to power loss. The power loss due to diode drop is a significant fraction of the overall harvested power (10–100 μW [3], [4]). It is, therefore, required for the diodes to conduct with minimum voltage drop. Hence, there is a need of a low-drop-diode equivalent (LDDE), which can be used to re-place the rectifier diodes. In particular, the LDDE should be able to replace the four diodes in full-wave bridge rectifier (FBR), as FBR is the most common circuit reported in the energy- harvesting literature, sometimes referred to as the standard [5].

The LDDE should meet the following requirements;

1) it should have a very low forward conduction drop;
2) it should block any reverse conduction;
3) it should be able to replace the four diodes in FBR;
4) it should not use an additional external power supply;
5) it should be powered directly from input signal and not from harvested power. This is to use the available input power instead of the extracted output power;
6) it should not demand additional off-chip components;
7) the control circuit should draw minimum power.

We propose an LDDE, which meets all of the aforementioned requirements. The LDDE is based on mimicking a low-drop diode with a MOSFET operated in linear region. Such a MOS- FET which is controlled such that it conducts in the deep triode region in one direction and goes into subthreshold region

(OFFstate) in the other direction is called a synchronous rectifier.

Previous implementations have also used synchronous rec- tifiers. However, their control circuit does not meet all of the aforementioned conditions 1–7. CMOS control rectifiers in [6]and [7] and the synchronous full-wave rectifier in [8] needan external power supply for powering up the comparator. Le *et al.*[8] also suggest a passive full-wave rectifier. It, how- ever, requires additional off-chip capacitors. It is also less power efficient owing to the continuous conduction of two diodes by drawing power from the output and also due to reverse conduc-tion by a transistor in saturation region. It also does not show the implementation in FBR.

In [9], a second piezoelectric patch is used to create two stable supply voltages to supply energy to a comparator. In [10], an additional input is required which is 180° out of phase with theinput for full-wave rectification.

The proposed LDDE can also be used in voltage multi- pliers [5], [11] and charge pump [12]. A voltage multiplier with output-powered active diodes is shown in [13]. In [14], a

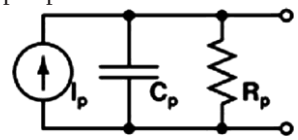


Fig. 1. Equivalent circuit of a PZD at resonance.

current-sensing approach is used for generating the gating sig- nals of output-powered comparator of the MOSFET-based ac-tive rectifier. Being output powered, diodes in both [13] and [14] consume standby power. In [15], a MOSFET-based full-wave rectifier followed by a diode to block reverse current conduc- tion is used. The diode is implemented as an active diode powered from the output. The circuit has greatly reduced the diode drop and improved the efficiency. However, the active diode consumes standby power. This issue has been taken careof, in [16] with an input-powered full-wave rectifier and ac- tive diode. In [5], the use of gate cross-coupled topologies of MOSFET-based FBR is indicated. This improves the power con-version efficiency. The ideas in [5] and [16] are specific to FBR implementation and are not of a stand-alone LDDE. The syn-chronous rectifier in [17] suggests a stand-alone LDDE. But itallows reverse conduction. Though the reverse current level canbe made small, it cannot be neglected when used in low-power circuits like vibration energy harvesters. There is also a resistor–diode (diode-connected MOSFET) path which is continuously conducting leading to power loss. Work in [17] and [18] has notbeen suggested for low power (10–100 μW) application.

In this paper, we have proved the efficacy of the proposed LDDE in a piezoelectric device (PZD)-based vibration energy-harvesting system. The electrical equivalent of a PZD [3] whenit is vibrated at its resonance frequency is shown in Fig. 1. I_p is a sinusoidal current source with amplitude equal to $I_{p\text{peak}}$. $I_{p\text{peak}}$ depends on the amplitude of vibration and the frequency f_p of the current source is equal to the frequency of vibration. Resonant frequency of the PZD is assumed to match with f_p. From Fig. 1, it is seen that the maximum available power from the PZD with conjugate matching of load is given by

When the rectifier–filter section is introduced at the output of PZD, it sets a further limit on the maximum available powerto the load. Let this limit on the maximum available or ex- tractable power be represented by $P_{\text{EXT}(\max)}$. Then, $P_{\text{EXT}(\max)}$ $P_{\text{PZD}(\max)}$.

≤

The proposed LDDE can replace the diodes in various ar-chitectures of rectifiers used for PZD-based harvesting. These architectures include conventional FBR, switch-only rectifier [3], [19], bias-flip rectifier [3], series synchronized switching harvesting with inductor (SSHI) [20], [21], synchronous charge extraction circuit [20], [22], voltage doubler [3], resonant recti- fier [23], and pulsed-resonant micropower converter [24]. Mak-ihara *et al.* [25] suggest SSHI with two rectification diodes instead of four. Series SSHI with magnetic rectifier [26] uses atransformer to reduce the effective diode drop by a factor equal to

TABLE I

$P_{EXT(max)}$ OF VARIOUS RECTIFIER ARCHITECTURES

Rectifier Architecture	$P_{EXT(max)}$ [3]
FBR	$C_p \cdot (V_p - 2V_D)^2 \cdot f_p$
Voltage Doubler	$C_p \cdot (V_p - V_D)^2 \cdot f_p$
Switch Only Rectifier	$2 \cdot C_p \cdot (V_p - V_D)^2 \cdot f_p$
Bias Flip Rectifier	$2 \cdot C_p \cdot (V_p - \frac{V_D}{Q})^2 \cdot Q \cdot f_p$
V_p is the open circuit voltage amplitude at the output of PZD. V_D is the rectifier diode drop. R_p is ignored in the derivation of $P_{EXT(max)}$ of the first 3 rectifiers. Q is qualitatively the parallel combination of the Q-factors of PZD and that of the resonant path of C_p and inductor of bias-flip rectifier.	

the transformer ratio. The $P_{EXT(max)}$ is dependent on the archi- tecture of rectifier. The SSHI and resonant architectures provide a high $P_{EXT(max)}$, as compared to the conventional FBR. Table Igives the $P_{EXT(max)}$ of different architectures. From Table I, it is seen that for all rectifier architectures, $P_{EXT(max)}$ increases as the rectifier diode drop decreases.

I. The remainder of this paper is organized as follows. Section IIcovers the working principle and power considerations of the proposed LDDE. Section III gives the design considerations and the simulation results in 130-nm technology. Section IV describes the detail of an experiment with the proposed LDDE,implemented with discrete components. Finally, Section V con-cludes this paper.

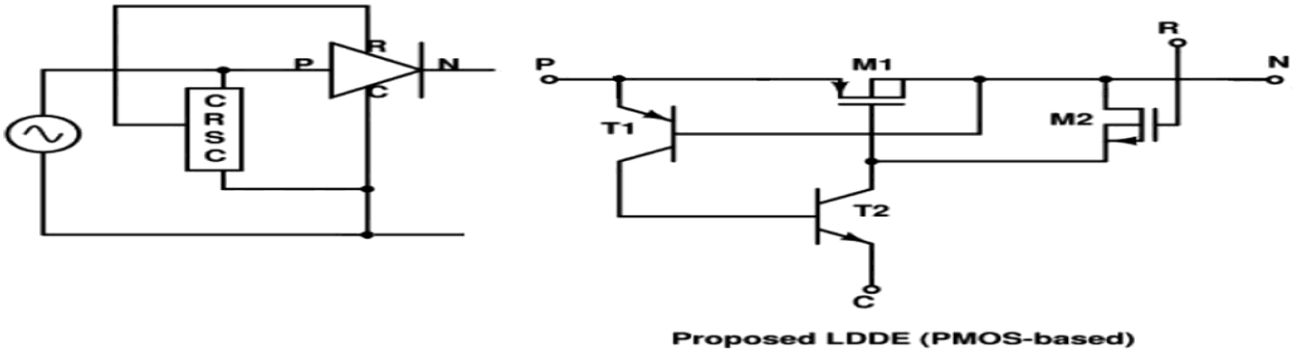
II. WORKING PRINCIPLE OF THE PROPOSED LDDE

A MOSFET operated in linear region (deep triode region) exhibits a very low value of dc resistance. It can conduct with lesser voltage drop for the same current, as compared to a diode or a diode-connected MOSFET (DCMOS). This property of MOSFET is exploited to use it to mimic a low-drop diode. It may also be noted that a DCMOS cannot be used as a low-drop diode, because of a minimum drop across it which is equal to the threshold voltage of MOSFET.

In the proposed LDDE, MOSFET is controlled such that it conducts only in one direction (call forward direction) andin linear region in the forward direction. A circuit diagram of the proposed LDDE is shown in Fig. 2. Source of PMOS (M_1) acts as the anode and drain of M_1 acts as the cathode of LDDE. The emitter–base junction of p-n-p transistor (T_1) is across (in parallel with) the source–drain of M_1. Substrate of M_1 is kept connected to drain to block reverseconduction.

To illustrate the LDDE operation, the following step-by-stepdescription is given:

1) When LDDE sees a voltage in the forward direction (pos- itive signal voltage), the emitter–base junction of T_1 is forward biased and T_1 begins to conduct.
2) When T_1 conducts, it provides the base drive current to n-p-n BJT (T_2) and T_2 enters into conduction.
3) The gate–source capacitance C_{gs} of M_1 gets connected across the PZD through T_2 and C_{gs} starts getting charged in the negative direction.



Proposed LDDE (PMOS-based)

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Circuit diagram of the proposed LDDE.

4)When the source–gate voltage V_{sg} of M_1 exceeds threshold voltage of M_1, M_1 starts conducting.

5)C_{gs} of M_1 continues to get charged and V_{sg} of M_1 keeps increasing. As V_{sg} keeps increasing, M_1 enters from the saturation region into linear region

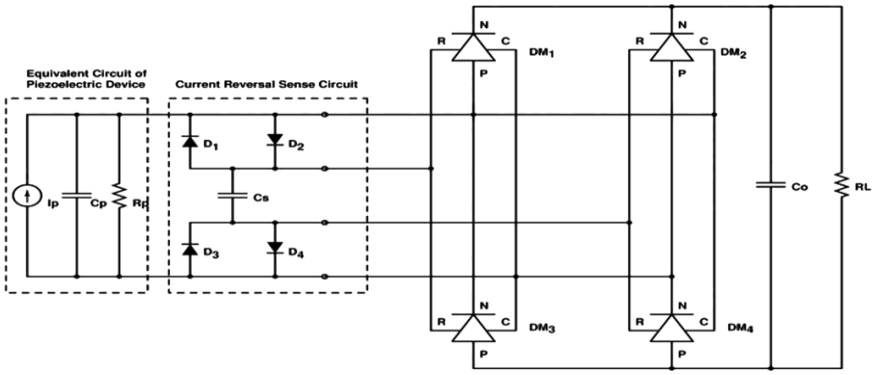
6) When M_1 enters the linear region of conduction, the source–drain voltage of M_1 (V_{sd}) reduces to a very low value.

7 When T_1 turns OFF, T_2 turns OFF.

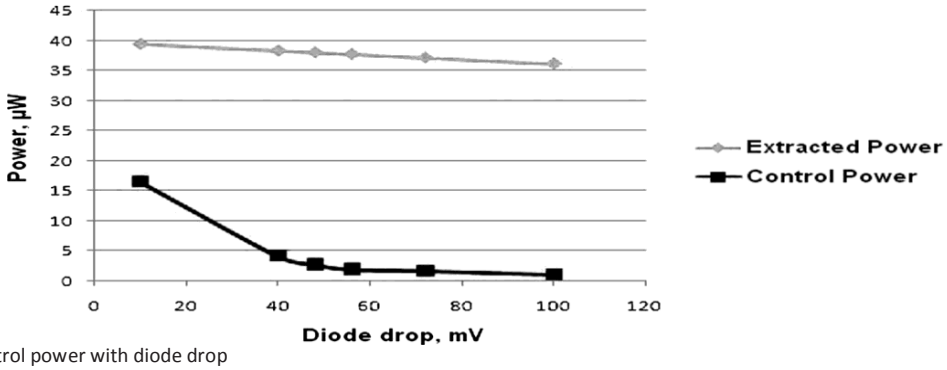
8.C_{gs} of M_1 stops getting charged. However, C_{gs} has no path to discharge and V_{sg} is maintained. This enables M_1 to continue conducting in the linear region. After M_1 starts conducting in the linear region, the drop across the paral-lel combination of M_1 source–drain and T_1 emitter–base junction is dictated by the linear region characteristic of M_1 . The drop across anode and cathode of the LDDE thus becomes equal to that across a MOSFET in linear region.

9.When signal reverses, signal R gets activated (generationof signal R is discussed shortly). Signal R is a one-diode-drop positive signal w.r.t cathode of LDDE (or anode of LDDE, cathode and anode being at almost the same po- tential).

10.Signal R turns ON the NMOS (M_2), which discharges C_{dg} of M_1 and turns M_1 OFF to prevent reverse conduction.



. FBR and filter for PZD using the proposed LDDE.



Variation of extracted power and control power with diode drop

III.Simulation Results

The circuit was simulated at an amplitude of $I_p (I_{p\,e\,a\,k}) = 60\ \mu$A. The optimum value of load resistance R_L, corresponding to the maximum output power, was determined by varying R_L and plotting output power, P_o versus R_L (see Fig. 8). Optimum value $R_{L\,op\,t}$ was determined to be 107 kΩ. All simulation results were taken at $R_{L\,op\,t}$, unless otherwise stated

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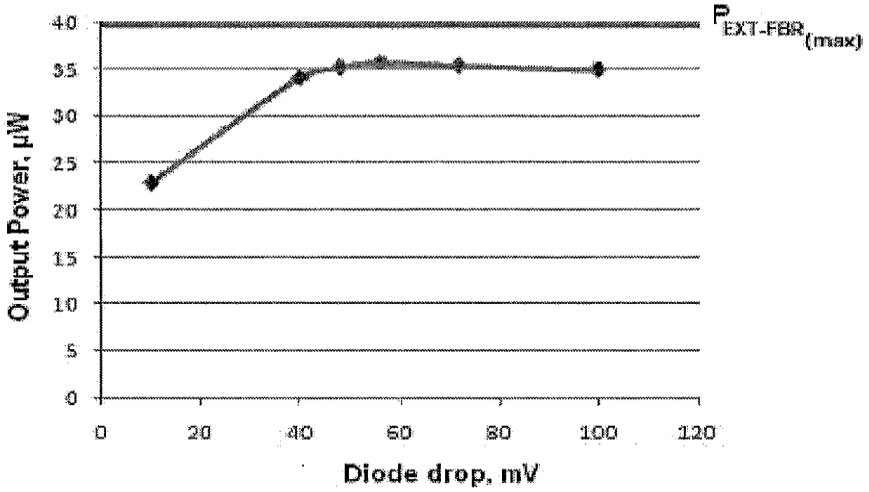

Fig. 7

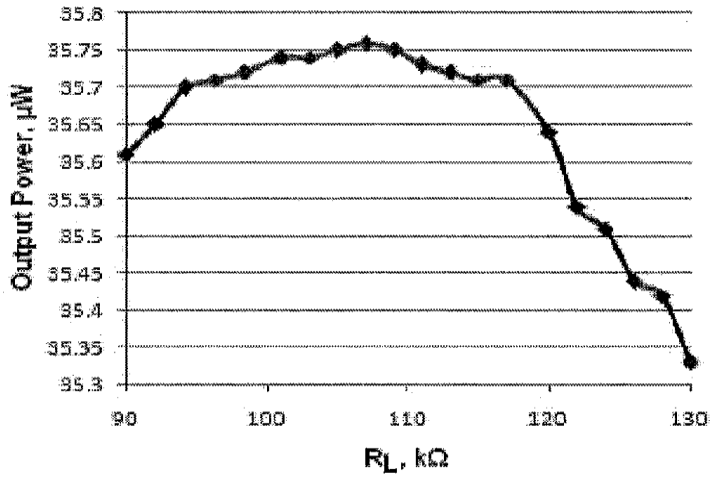

Fig. 8

FIG. 7 shows that the power P_o maximizes at a diode drop of 56 mV. Also, T_1 is a set of parallel BJTs and the number of T_1s is based on the number of T_2s.

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The circuit is developed/simulated and tested at an amplitude of I_p (Ip_{peak}) equal to 60 μA. The optimum value of load resistance R_L, corresponding to the maximum output power is determined by varying the resistor R_L and finding the output power P_o.

FIG. 8 illustrates a plot of P_o versus R_L or the variation of output power with load resistance. The optimum value RL_{opt} was determined to be 107 kΩ.

The output power P_o is calculated by measuring V_o as

$$P_o = V_o^2 / R_L \quad (4)$$

The circuit is developed/simulated at various values of Ip_{peak}. The LDDE forward conduction drop V_D, LDDE current, gate control voltage of LDDE, and output voltage V_o are plotted as shown in FIGS. 9 and 10.

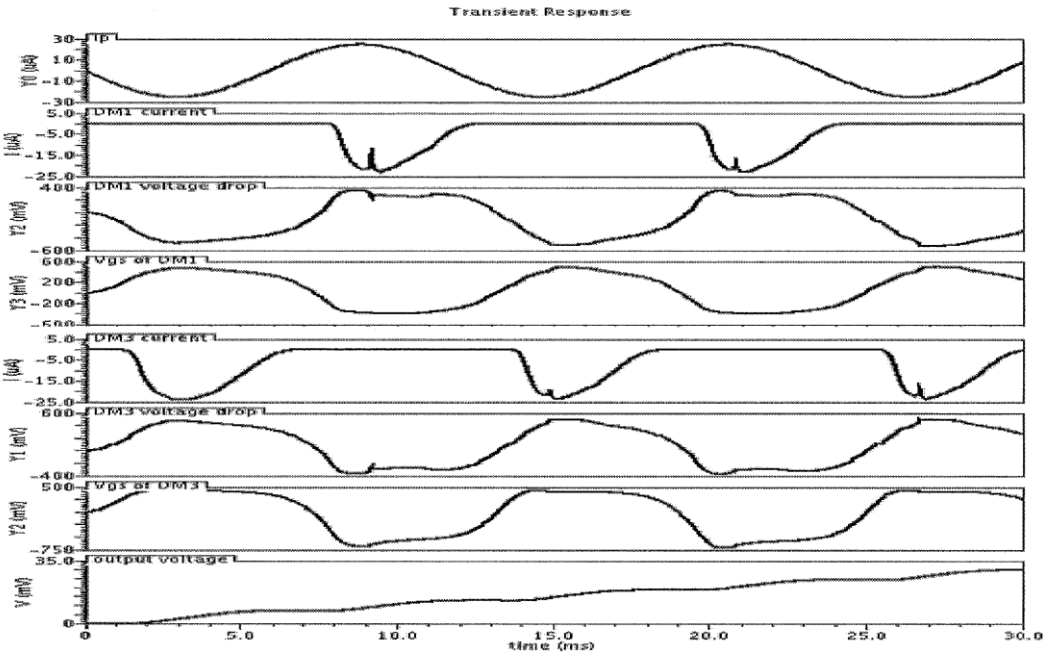

Fig. 9

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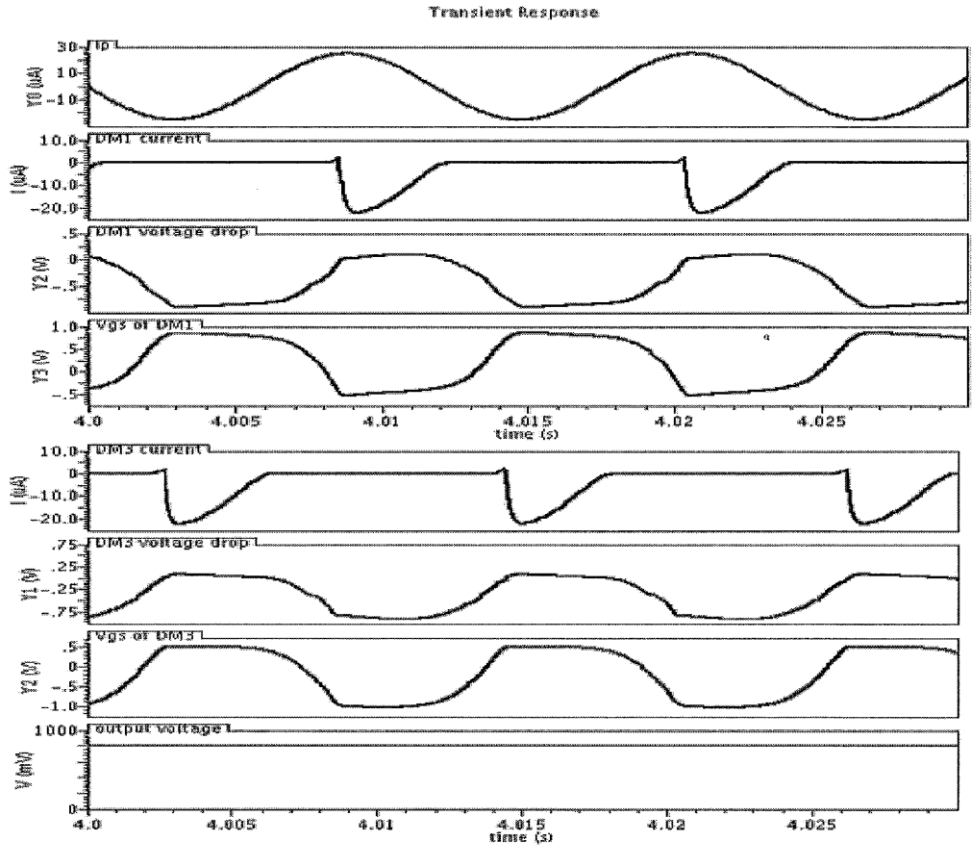

Fig. 10

TABLE II

P_O AND η OF LDDE-BASED FBR AT VARIOUS VALUES OF $I_{p_{peak}}$

$I_{p_{peak}}$ (μA)	V_p (V)	$P_{EXT-FBR_{(max)}}$ (μW)	P_o (μW)	η (%)
20	1.413	4.41	3.71	84.13
30	2.122	9.95	8.83	88.74
40	2.828	17.67	15.55	88.00
50	3.535	27.62	24.38	88.27
60	4.241	39.75	35.76	90.0

When not in the deep triode region, conduction loss is themajor loss. As R_L increases for a fixed $I_{p_{peak}}$, V_o increases, V_{gs} increases, V_D decreases, and, hence, conduction loss decreases with the increase in R_L. The decrease in conduction loss is alsodue to the lesser conduction period as R_L increases. Also, whennot in the deep triode region, as $I_{p_{peak}}$ increases at a fixed R_L, V_o increases, V_{gs} increases, V_D decreases at a faster rate than$I_{p_{peak}}$increases, and thus conduction loss decreases.

When M_1 enters into the deep triode region, switching lossdominates. For a fixed R_L, as $I_{p_{peak}}$increases, V_o increases, V_{gs} increases, and switching loss increases. The conduction loss

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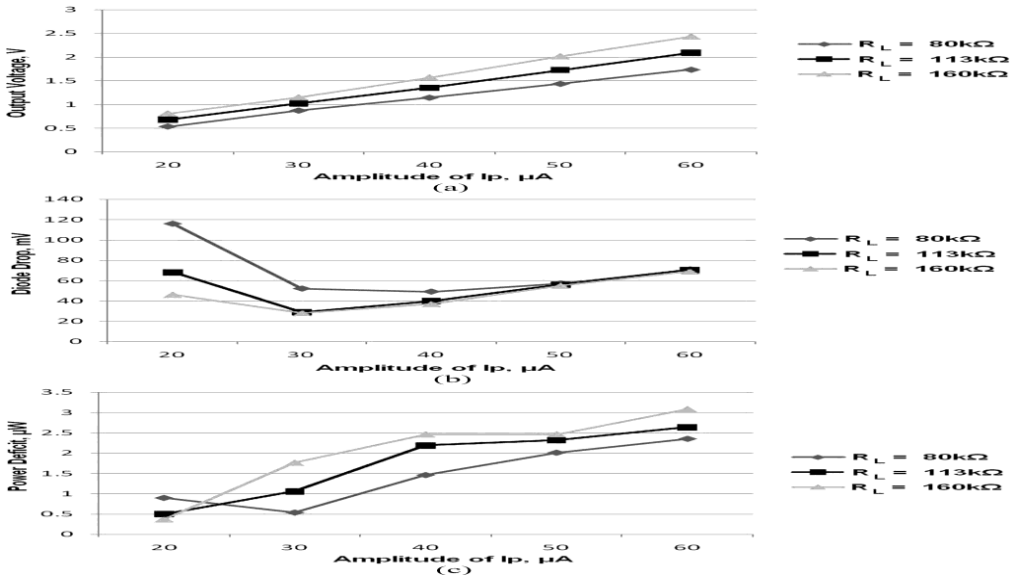

Fig. 11. Performance of LDDE-based FBR as a function of $I_{p\,peak}$ for various

R_L. (a) Output voltage. (b) Diode drop. (c) Power deficit.

also increases, as in the triode region, V_{ds} increases with I_{ds} (or $I_{p_{peak}}$). For a fixed $I_{p_{peak}}$, as R_L increases, V_{gs} increases leading to higher switching loss. The variation in V_{ds} (or V_D) with R_L is insignificant in the deep triode region.

For comparison with the standard DCMOS, the FBR-filter section of PZD was wired with DCMOS and simulated. The DCMOSs used were of the same type and dimension, as M_1 (see Fig. 2) of LDDE, to enable the best comparison. $R_{L_{opt}}$ of DCMOS-based FBR was found to be 111 kΩ.

Figs. 12 and 13 show that the LDDE scores over DCMOS both in terms of lower V_D and higher P_o. P_o is higher by upto 169% for low values of $I_{p_{peak}}$ and by up to 30% at higher values of $I_{p_{peak}}$. This trend can be understood from $P_{EXT_{(max)}}$ of FBR, as given in Table I.

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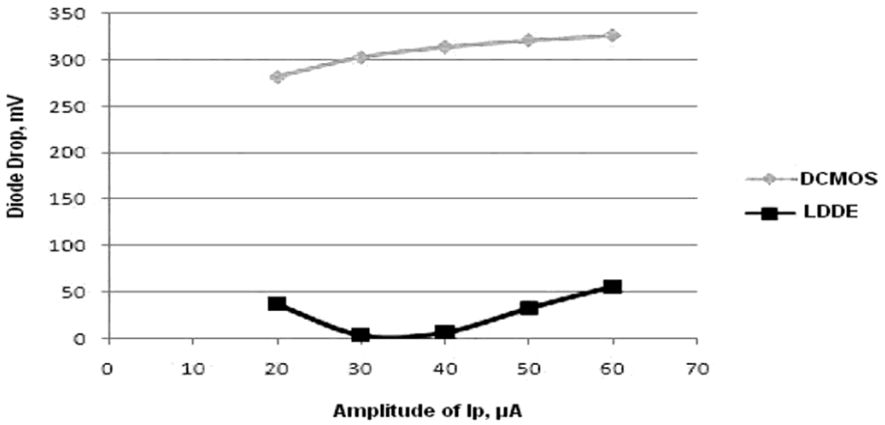
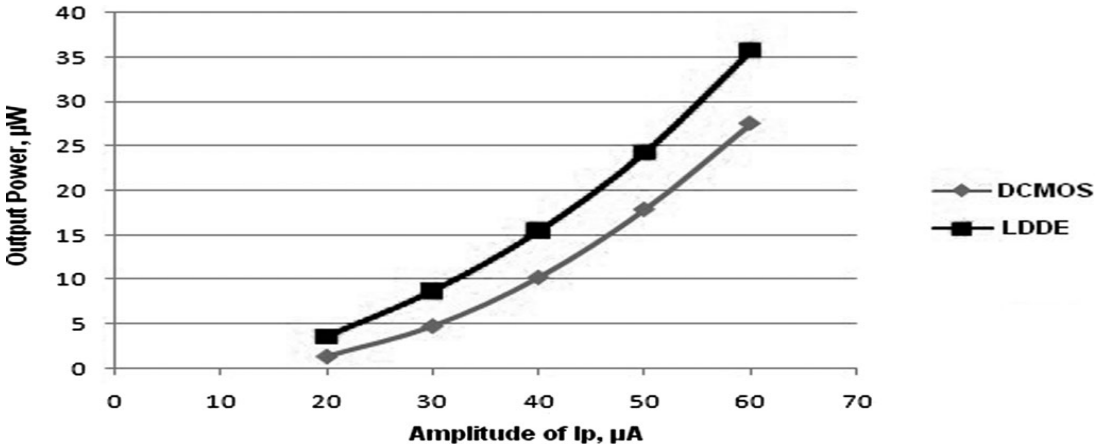


Fig. 12. Comparison of diode drop of LDDE with that of DCMOS.



IV.EXPERIMENTAL VERIFICATION

The FBR-filter section of the interface circuit for PZD-based vibration energy harvesting was rigged up using discrete com- ponents. Specified working of the proposed LDDE was verified by wiring it up using discrete components and using it in place of the four diodes in FBR. To enable comparison with the conventional DCMOS, the FBR-filter was configured, both using the proposed LDDE and conventional DCMOS.

A. PZD Detail

The PZD used was Mide Volture V21BL. It has two piezoelec- tric strips on the same substrate, but with independent electrical wiring. Each strip has a C_p of 26 nF.

B. FBR Circuit Details

The LDDE-based FBR was configured using discrete com- ponents, as shown in Table IV. The DCMOS-based FBR was configured using the same type of MOSFET as used for LDDE-based FBR to enable the best comparison.

C. Experimental Setup

The PZD was mounted along the datasheet-specified clamp line in a cantilevered configuration on the LDS Dactron shaker, as shown in Fig. 14. The two electrical wires corresponding to one of the piezostrips were taken out and connected to the input of FBR. The wires taken out were arrested properly after giving them enough stress relief. The voltage across different points in the circuit was measured using a digital storage oscilloscope.

The LDS Dactron Shaker gives calibrated sinusoidal vibration in the vertical direction at user-set frequencies and amplitudes (given in terms of acceleration *g*).

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D. Measurement Results

1) *Determination of resonance frequency of PZD:* The PZDwas vibrated at various frequencies from 50 to 500 Hz at afixed amplitude of 1*g*. The amplitude of sinusoidal outputfrom PZD peaked at 85 Hz. Resonance frequency =85 Hz.

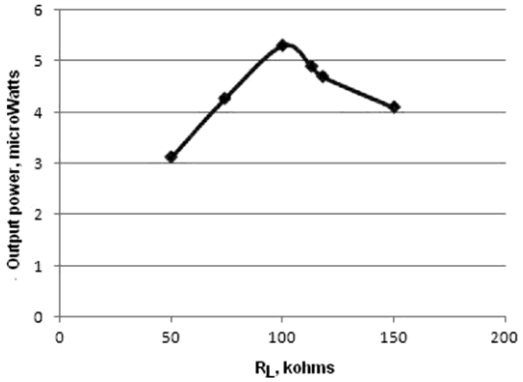

Fig. 15. Variation of the proposed LDDE-based FBR output power with loadresistance (frequency of vibration = 85 Hz; acceleration = 0.5*g*).

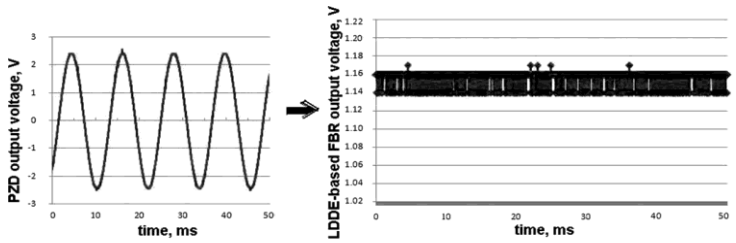

Fig. 16. Output of LDDE-based FBR at 0.8*g*, 85 Hz vibration of PZD(reproduced from digital oscilloscope-recorded data points). (a) PZD output.

(b) FBR-filter output.

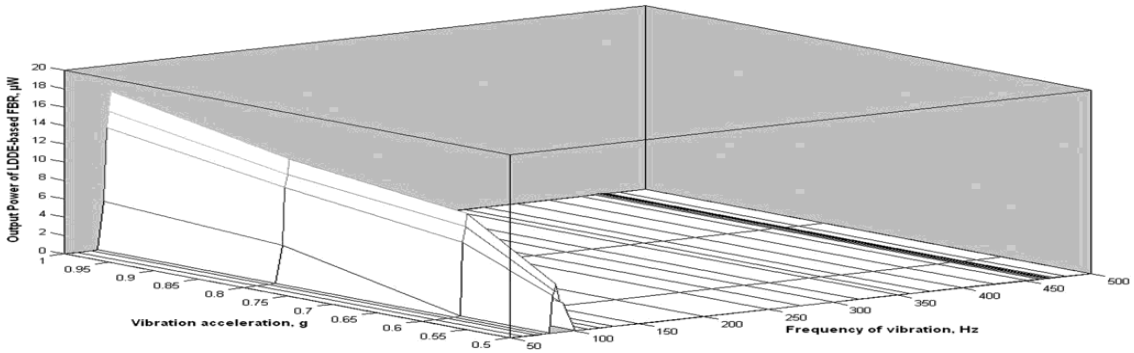

Fig. 17. Output power of LDDE-based FBR at different frequencies and am-plitudes of vibration of PZD

1) *Determination of optimum load for the PZD-rectifier cir-cuit:* The PZD was vibrated at 85 Hz, 0.5 g, and the output voltage V_o from the FBR filter was noted at various values of load resistance R_L . Output power P_o in each case was calculated from (4). Output power peaked at R_L =100 kΩ (see Fig. 15). Optimum load resistance = 100 kΩ. R_L was kept fixed at its optimum value during the rest of the experiment.

Characterization of LDDE-based FBR: The PZD was vibrated at various frequencies from 50 to 500 Hz and amplitudes from 0.5*g* to 1*g*. The output voltage $V_{o\,of}$

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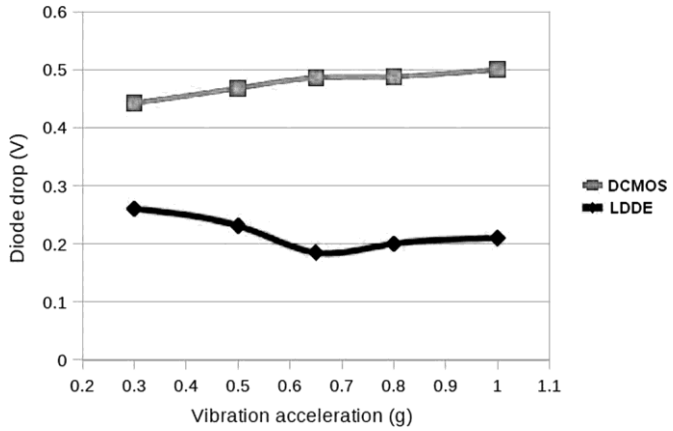
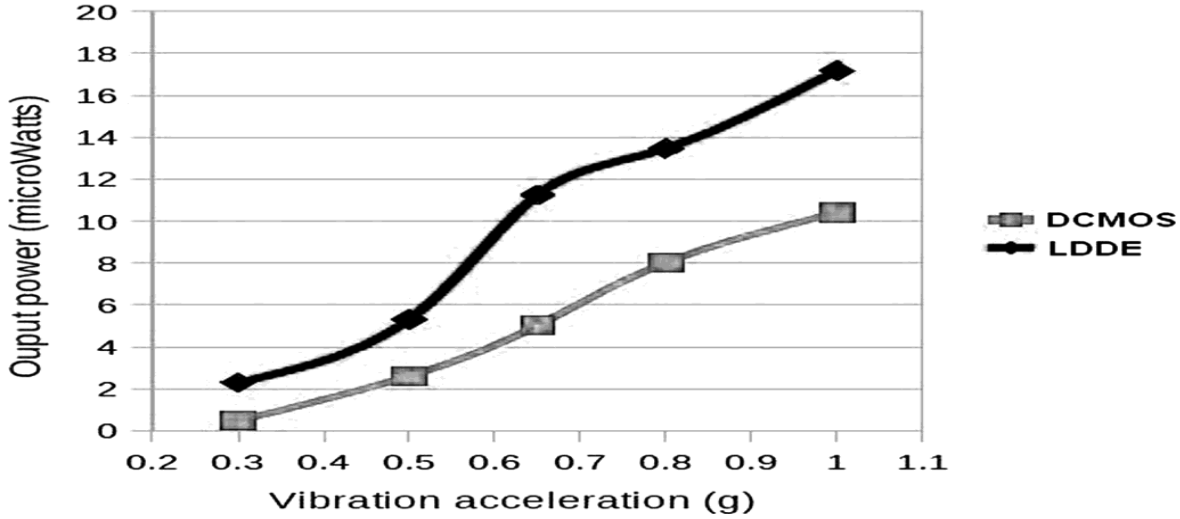


Fig. 18. Comparison of forward conduction drop of LDDE with DCMOS(Vibration Frequency = 85 Hz).



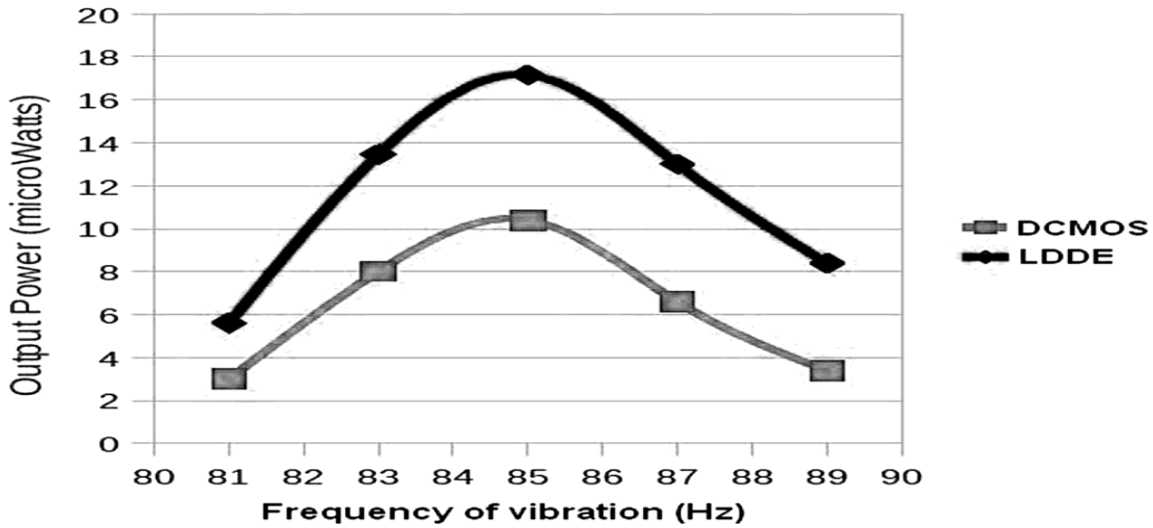


Fig. 20. Comparison of output power from LDDE-based FBR with that fromDCMOS-based FBR (Vibration acceleration = 1*g*).

LDDE-based FBR was measured (see Fig. 16) and recorded in each case. The output power was

calculated from (4). A 3-D plot of output power was made based onthese data (see Fig. 17).

2) *Comparison of performance of LDDE with that of DC- MOS:* The PZD was vibrated at various frequencies from 81 to 89 Hz and amplitudes from 0.3*g* to 1*g*. Rectified voltage at the optimally loaded output of FBR and the diode drop were measured in both the configurations, viz., LDDE-based and conventional DCMOS-based. Out-put power was calculated using (4).

Figs. 18–20 show that the proposed method has a strict ad- vantage over conventional method in terms of lower diode dropand higher output power, under same input conditions.

In general, the LDDE-based FBR provided a 65–104% in- crease in power as compared to the DCMOS-based FBR

V. CONCLUSION

A linear region-operated-MOSFET-based LDDE has been proposed. It can be directly powered from input signal and requires no additional power supply. The proposed diode equiv- alents have been used to replace the four diodes of FBR in PZDinterface circuit. The efficacy of the proposed diode in decreas-ing the diode drop and increasing the output power from a PZD- bridge rectifier circuit has been demonstrated through simula- tion in 130-nm technology and experiment with discrete compo- nents. It provides a 30–169% increase in output power as com- pared to a bridge rectifier with conventional diode-connected MOSFETs. The simulation in 130-nm technology also shows that it can extract 90% of the maximum available power from an ideal PZD-bridge rectifier circuit. Setting aside the constraint of power loss, simulations indicate that a diode drop as low as 10mV at 38 μA can be achieved.

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