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Design of Efficient 32-bit Ripple Carry Adder Using Reversible logic gates

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Abstract: This project outlines the RCA (Ripple Carry Adder) which has the simplest structure with the smallest area and power consumption but with the worst critical path delay. In the CSLA(Carry Select Look Adder), the speed, power consumption, and area usages are considerably larger than those of the RCA.

There are different types of the parallel prefix algorithms that lead to different PPA structures with different performances. As an example, the carry save adder (CSA) is one of the fastest structures but results in large power consumption and area usage. It should be noted that the structure complexities of PPAs are more than those of other adder schemes. The CSKA, which is an efficient adder in terms of power consumption and area usage, but the critical path delay of the carry skip adder (CSKA) is much smaller than the one in the RCA, whereas its area and power consumption are similar to those of the RCA. In addition, the power-delay product (PDP) of the CSKA is smaller than those of the CSLA and PPA structures.

The comparatively lower speed of this adder structure, limits its use for high-speed applications. In this paper, given the attractive features of the CSKA structure, we have focused on reducing its delay by modifying its implementation based on the static CMOS logic.

Index Terms: PPA, CSLA, CSKA, RCA, power consumption and critical path.

I Introduction:

Adders are a key building block in arithmetic and logic units (ALUs) and hence increasing their speed and reducing their power/energy consumption strongly affect the speed and power consumption of processors. There are many works on the subject of optimizing the

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speed and power of these units, which have been low-power/energy consumptions, which is a challenge for the designers of general purpose processors.

One of the effective techniques to lower the power consumption of digital circuits is to reduce the supply voltage due to quadratic dependence of the switching energy on the voltage. Moreover, the sub threshold current, which is the main leakage component in OFF devices, has an exponential dependence on the supply voltage level through the drain-induced barrier lowering effect. Depending on the amount of the supply voltage reduction, the operation of ON devices may reside in the super threshold, near-threshold, or sub threshold regions. Working in the super threshold region provides us with lower delay and higher switching and leakage powers compared with the near/sub threshold regions.

In the sub threshold region, the logic gate delay and leakage power exhibit exponential dependences on the supply and threshold voltages. Moreover, these voltages are (potentially) subject to process and environmental variations in the nano scale technologies. The variations increase uncertainties in the aforesaid performance parameters. In addition, the small sub threshold current causes a large delay for the circuits operating in the sub threshold region.

Recently, the near-threshold region has been considered as a region that provides a more desirable trade off point between delay and power dissipation compared with that of the sub threshold one, because it results in lower delay compared with the sub threshold region and significantly lowers switching and leakage powers compared with the super threshold region.

In addition, near-threshold operation, which uses supply voltage levels near the threshold voltage of transistors, suffers considerably less from the process and environmental variations compared with the sub threshold region.

The dependence of the power (and performance) on the supply voltage has been the motivation for design of circuits with the feature of dynamic voltage and frequency scaling. In these circuits, to reduce the energy consumption, the system may change the voltage (and frequency) of the circuit based on the workload requirement. For these systems, the circuit should be able to operate under a wide range of supply voltage levels. Of course, achieving higher speeds at

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lower supply voltages for the computational blocks, with the adder as one the main components, could be crucial in the design of high-speed, yet energy efficient, processors.

In addition to the knob of the supply voltage, one may choose between different adder structures/families for optimizing power and speed. There are many adder families with different delays, power consumptions, and area usages. Examples include carry save adder (CSA), carry skip adder (CSKA), and carry select adder (CSLA).

II Existing Work or Literature Survey:

Reversible logic is logic which produce no heat dissipation. Because the amount of energy dissipated in entire block is directly proportional to the number of bits erased during the process of the computation, if the circuit is designed in such a way that there is no information loss then it is called as reversible. Reversible circuits are designed using reversible logic gates. Reversible gate will produce unique output vector for each set of input vector applied and with the help of quantum primitive gates, a new reversible gate is designed.

The designed new gates will have the ability to produce all conventional logical operations like AND, NAND, OR, NOR, XOR, XNOR. The design of the full adder is made by using newly proposed SMG Gate. The newly proposed gate is more efficient than the other full adder circuits. For each bit of information lost produces k*T*log2 Joules of energy, where k is Boltzmann‟s constant and T the absolute temperature where the operations are being performed. To perform some computations in conventional system some millions of transistors are used.

The advantages of using reversible logic gates in the implementation of circuits is it decreases garbage outputs, number of gates utilized. The results are compared with circuits which are made with conventional gates. The newly proposed adder/subtractor circuit can be applied vastly in the design of the nanotechnology which has wide applications. The reversible logic has emerged as a promising technology and have applications in quantum computation.

III Proposed Work:

Proposed design of Carry Select Adder compares the power dissipation with the existing work. They presented the design of Carry Select adder using TSG module. Ripple carry adder is one

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of the efficient adders which is easy to design and also easy to analyze but slow in processing. In order to achieve much more speed using carry look a-head adder is advisable but major drawback of this is consumes more area and power dissipation.

By keeping these two major drawbacks, carry select adder is advisable These stages are arranged in a binary tree structure to generate a sum and carry with reversible multiplexers which has less quantum cost and less area when compared with conventional gates.

IV Results:

This paper presents the design and simulation of 16 bit efficient ripple carry adder using reversible logic gates. In reversible logic gates there is no information loss and zero heat generation.So by using reversible logic gate we can reduce the power dissipation.

The performance of Ripple Carry Adder circuits can be improved using reversible logic and evaluate the number of gate count, garbage output, quantum cost and delay of the Ripple carry adders implemented using Reversible logic gates. Reversible circuit design strategy is used to reduce the complexity and circuit cost. Distinguish the circuit with reversible systems, which performs more number of complex operations. Based on the reversible circuit design main factors like garbage outputs, quantum cost and delay of the circuit are reduced.

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