JOURNAL OF CRITICAL REVIEWS

ISSN- 2394-5125 VOL 07, ISSUE 19, 2020

LOW-POWER CORRELATORS FOR EFFICIENT SPECTRUM SENSING IN AERONAUTICAL-LDACS COMMUNICATION SYSTEMS

P Surendrababu[1], Dr.Vijay Prakash Singh [2]

[1]Research Scholar , Dept. of Electronics and Communication Engineering,Sri Satya Sai University of Technology and Medical Sciences, Sehore Bhopal-Indore Road, Madhya Pradesh, India

[2]Research Guide, Dept. of Electronics and Communication Engineering ,Sri Satya Sai University of Technology and Medical Sciences

---

Abstract

The increase in aviation traffic over the past ten years has increased the demand for improved air traffic management strategies. A well known framework that attempts to take utilization of contemporary computerized communication techniques and figuring models is the L-band Advanced Aeronautical Communication Framework (LDACS). To increment range economy and communication limit, mental radio-based strategies have additionally been proposed for LDACS; by and by, these call for modern process capacities in airplanes that implement severe space and power limits. This study recommends coordinating multiplier less connection into the on-board LDACS framework to empower range detecting in LDACS air-to-ground communications. A creating standard called L-band advanced aeronautical communication framework type-1 (L-DACS1) plans to further develop air traffic the executives by supplanting the obsolete relationship aeronautical communication frameworks with the improved and exceptionally dependable compelling computerized climate. In contrasted with the ongoing aeronautical communication frameworks, L-DACS1 utilizes a contemporary and compelling symmetrical recurrence division multiplexing (OFDM) regulation way to deal with produce an additional effective and higher information rate.

Keywords: *Low-Power, Correlators, LDACS, Communication*

1. INTRODUCTION

The Global Common Flight Association (ICAO) has proposed the Future Communications Foundation as an answer for this issue. This foundation would consolidate the best information interface conventions for helping aerial, air-to-ground, and satellite-based network. (17, 2007.) L-band Computerized Aeronautical Communications Framework (LDACS) is turning out to be more famous as the picked answer for extreme arrangement for air-to-ground linkages As LDACS is imagined as an overlay strategy for existing L band frameworks, for example, Distance Estimating Gadgets, it has demanding standards for both transmission and gathering rather than the traditional relationship approaches utilized by present frameworks, LDACS utilizes state of the art advanced tweak calculations like Symmetrical Recurrence Division Multiplexing (OFDM) for upgraded execution and range effectiveness. (Kamali, 2010)The interest for traveller air traffic is supposed to twofold from its ongoing level by around 2025, following twenty years of continuous industry development. The present-day air transportation framework will not have the option to deal with this turn of events, for instance, Europe's as of now restricted very high-recurrence communication limit is anticipated to arrive at immersion by 2020-2025. (Challenges of growth 2008 summary report, 2008)To meet these extending needs, viable air-to-ground communication frameworks that can convey an assortment of airplane information continuously are required. The L-band computerized aeronautical communication framework (L-DACS), which plans to explore advanced radio innovation to empower powerful communication for cutting edge worldwide ATM frameworks, is being advanced as an answer that can coincide with existing L-band frameworks. Two guidelines for L-DACS are being analyzed: type 1 (L-DACS1) and type 2. (L-DACS2). The sort 1 definition

The top and possible contender for extreme determination is the Advanced Article Identifier 10.1109/TVLSI.2018.2789467 as laid out by EUROCONTROL [4]. L-DACS1 is intended to work in the 960-1164 MHz recurrence band, which is fundamentally utilized by aeronautical route helps [such as TACAN and DME for military strategic air route (TACAN)]. (Diaz et al., 2015.)Because of the huge number of L-band frameworks currently set up, doling out additional spectrums could challenge. An engaging strategy is the trim procedure, where L-DACS1 is worked in the ghostly holes between two adjoining DME or TACAN channels.

With this procedure, the ongoing apportioned range for any remaining L-band frameworks might be kept without the requirement for any extra range allotment.

The trim methodology, in any case, raises an extraordinary obstruction issue. It is fundamental that the L-DACS1 collector be impervious to impedance from other L-band frameworks. (Rech, 2016) Symmetrical recurrence division multiplexing (OFDM) regulation, which has been generally utilized in an assortment of high bit rate remote transmission frameworks, is utilized in L-DACS1 (e.g., WiMAX and WiFi). Thus, L-DACS1 can arrive at a more prominent information throughput while being more successful than the ongoing ATM frameworks. With its advantages of diminishing imprudent clamour, strength to multipath impacts, and unearthly proficiency, OFDM is a contemporary and productive multicarrier balance innovation. Sadly, recipient synchronization influences how well OFDM performs. Inter symbol obstruction (ISI) can result from fleeting synchronization issues and transporter recurrence offset, separately. (F. Shamani, 2014)Accordingly, synchronization is vital for the usefulness of OFDM frameworks like L-DACS1.

2. REVIEW OF LITREATURE

Seo & Kim (2010) created a MAC unit that combines multiplication and accumulation to handle high-speed math. This facilitates the creation of a hybrid carry-save adder using a modified Booth's algorithm based on one's complement. In addition, it has a sign extension function that increases the bit density of the operands. (F. Shamani R. A., 2017.)The combination of pipelining and synthesis in the suggested architecture results in increased MAC performance that is twice as good as that of prior studies, in addition to 90 nm CMOS library, which is done in 250, 180, and 130 m. STA analysis is eventually completed for validation.

Francis et al. (2013) developed a Braun multiplier to multiply arrays in parallel. Using bypassing methods and adder modifications for the purpose of minimizing latency and power consumption, this multiplication is performed on the unsigned values. Optimised adders are used in place of full adders in the ripple carry adder final stage. (J. S. Park and T. Ogunfunmi, , 2012.)Double-pass transistor logic (DPL) and transmission gate (TG) logic can be used as optimal adders. Braun multiplier is implemented using 0.13um CMOS technology and is combined with several logic type adders. The performance characteristics of various adders have been compared, and the Braun multiplier with column bypass has produced better outcomes.

Abdelgawad (2013) a quick and low-power MAC unit was built for WSN applications. By combining MAC designs' critical delays and hardware difficulties, the MAC unit is realized here with little hardware complexity and minimal critical route delay. Simplifying the hardware of the summation network reduces overall performance. Instead of distributing the bits of the collected operands across the network, the add tree receives them before the final adder, increasing the speed of operation. (L. Hanzo and T. Keller, , 2006.) When 32-bit MAC unit is developed utilizing ASIC technology, about 5.5% Area, 9% Energy, and 13% Delay reduction are attained.

Kuo & Chou (2010) used a row bypassing approach to create an array multiplier with minimal power and fast speed. To reduce power consumption, the multiplier's adders with zero input are deactivated. Using parallel architecture is mostly used to reduce delay time. Using standard TSMC 0.18 mm CMOS technology, Cadence Spectre is used for post-layout simulation, during which the Delay and Power consumption are calculated in order to verify the design efficiency. (M. Sajatovic, , 2011.) For both signed and unsigned multiplication processes, high power-efficiency is obtained with a modest increase in the hardware and Power-Delay product.

Fayed & Bayoumi (2002) presented a high-speed multiply accumulate unit to accelerate VLSI systems' signal processing. In this design, binary trees created using 4-2 compressor circuits are used. For extemporizing operating speed, 4-2 compressors' free input lines are used. The partial products create free input lines in the form of a parallelogram. With the merging of operations throughout the multiplication process, the gaps are filled using the collected bit values. Prototyping an 8-bit multiplier accumulator in 0.35 micron dual-metal CMOS. The 4.26 ns delay shown in this design corresponds to a reduction of 16.8 μs. Power consumption at 150 MHz is approximately 324 mWatt. This reduces performance by 23.04%.

Malleshwari & Srinivas (2016) developed 64 bit MAC architecture for a summation network to conduct addition and multiplication operations simultaneously. The suggested architecture and the combined architecture have been compared. The combined architecture takes full advantage of summation trees. The collected data bits were sent to: Two unused inputs to the compressor. This combination of accumulation and multiplication reduces the cost of an additional accumulator. The free inputs are filled by using 5:2 compressor methods. It is employed to reduce the area of the recommended 64 bit MAC architecture. With the removal of critical paths, the MAC structure in this study achieves a 21.9% area

reduction, a 75.7% power reduction, and a 12% delay reduction. This 64 bit MAC is created using Veri log HDL in Xilinx ISE14.3i on the Zynq FPGA development board.

3. LDACS MULTIPLIERLESS CORRELATOR FOR SPECTRUM SENSING

3.1 Architecture of Multiplier less Correlator

Without technical improvements, running such a jumbled cross- Correlators on a running FPGA would result in a high DSP block requirement of 1500 blocks in addition to registers, increasing both static and dynamic power usage. would require a very large device that increases the updated plan uses the DSP block's internal pipeline registers to absorb the delay stages, reducing the amount of detail (registers/LUTs) that need to be used while reducing the overall framework execution (clock speed) can be improved. A similar DSP block might be reused all through two estimations in an asset obliged execution to slice the usage down the middle, yet doing so would raise idleness at every hub by 4 while as yet utilizing more power. (N. Lashkarian and S. Kiaei, 2000) The DSP blocks could on the other hand be time-multiplexed through multi-siphoning However; this requires higher clock speeds and consumes more power. By exchanging a multiplier or multiple multipliers for a series of shift additions, the multiplier-less relation limits this complexity while using fewer registration resources at the expense of accuracy.

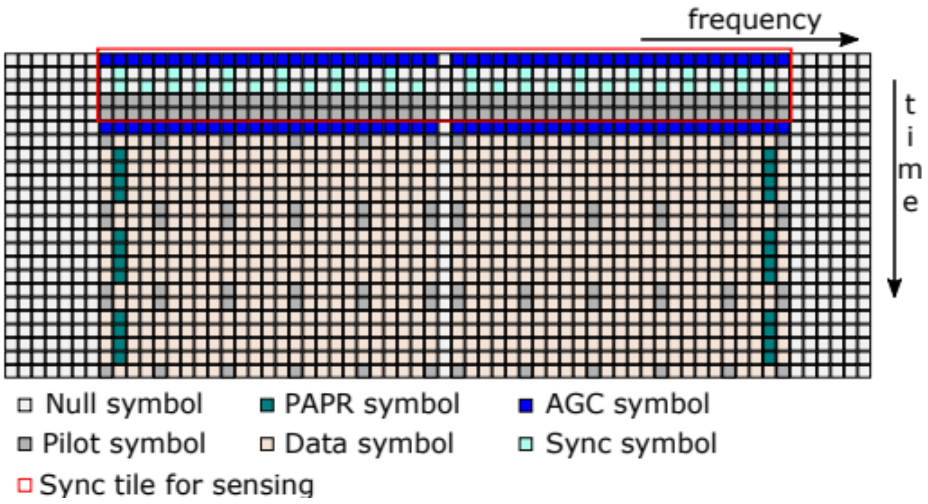


Figure 1: Reproduced RL DC Segment Organization

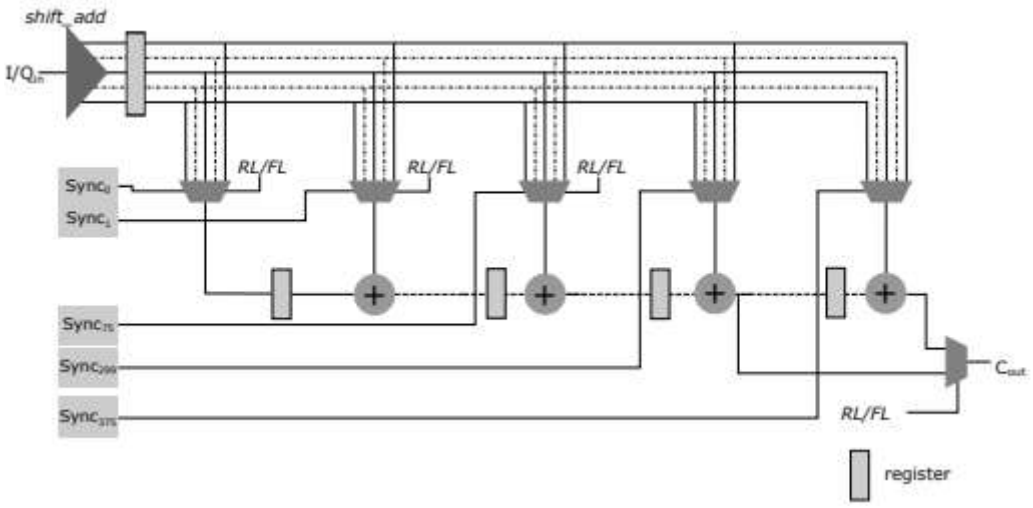


Figure 2: The multiplier less correlator's architecture

The multiplier less correlator broadens the correlator utilized in for the IEEE 802.16d norm and its undeniable level plan is portrayed in Fig. 3. The construction looks like a transpose direct structure channel, however rather than performing increase at each tap, a multiplexer picks one of its various information sources in light of the worth of the synchronization signal at that tap (Sync[n]). (T. H. Pham, 2017)Like, our design upgrades asset use by utilizing a solitary common shift-add block; nonetheless, our methodology empowers more prominent quantization levels to improve execution within the sight of very low SNR. This normal shift-add block figures generally possible products of the information test comparing to the 375 synchronization tests subsequent to getting the I and Q parts from the RF front-end.

A lengthy critical route passes via the multiplexers in LDACS due to the long synchronisation tile, whereas the architecture in employs a 64 sample preamble structure. To counteract this, we raise the design's operating frequency by adding a pipeline step at the tap multiplexers' output. Finally, the information multiplexers for taps 1-75 contain an additional select line. This bypasses the shift-add input of '0' to the correlators and allows synchronizing the FL outlines (interesting for the application). Synchronized images are reused individually rather than as a whole tile. In this case synchronization is achieved by the result of tap 225.

Signal to noise ratio (dB)	Failure rate (%)
10	2.3
24	2.5
31	3.6
35	3.9

41	4.2
46	4.6
51	5.1

Table 1: Variation in multiplier less correlator quantisation settings for LDACS-1 frame detection accuracy.

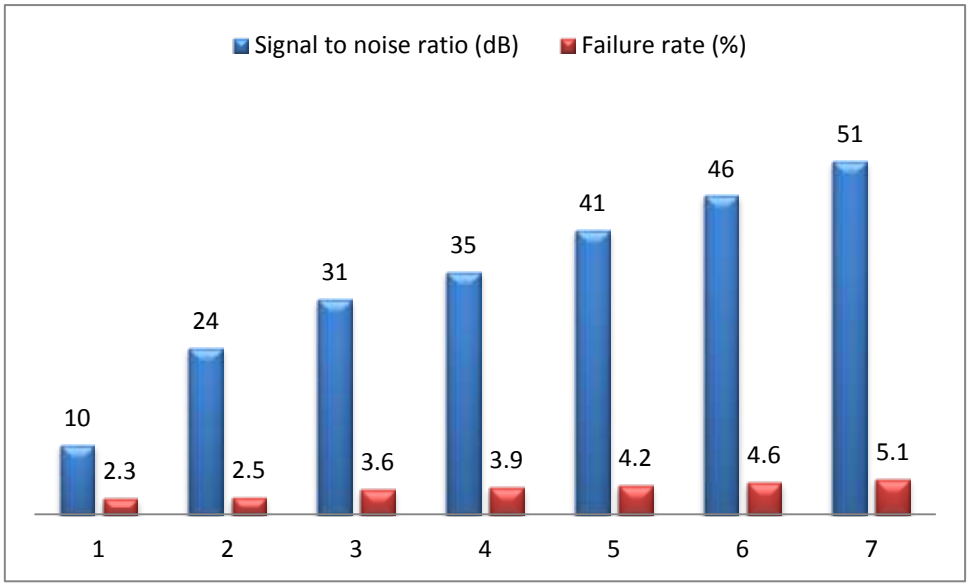


Figure 3: Variation in multiplier less correlator quantisation settings for LDACS-1 frame detection accuracy.

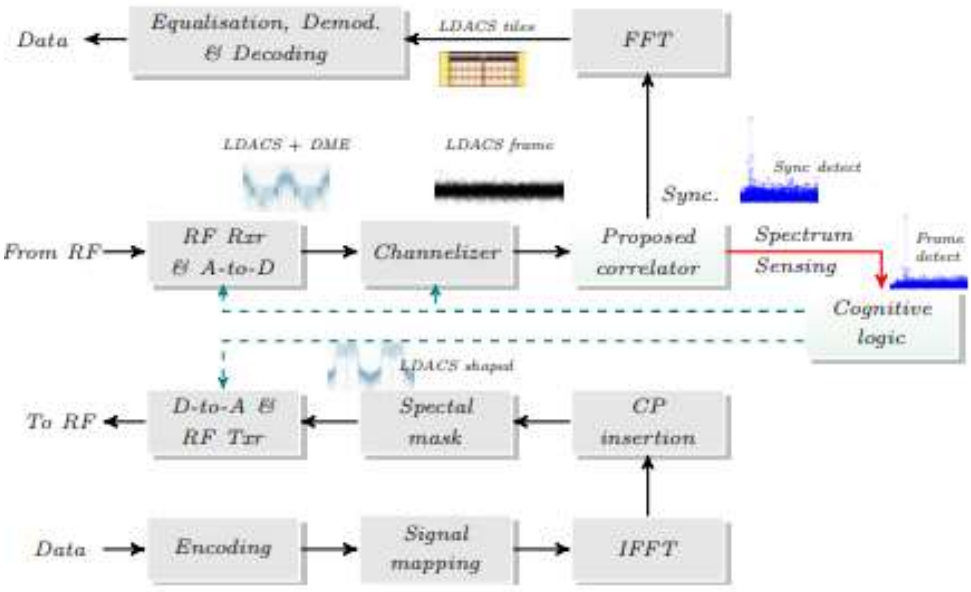


Figure 4: Include the multiplier less correlator in the LDACS pipeline.

3.2 Correlator proposed for the LDACS processing chain

The LDACS baseband is portrayed in an improved on block chart in Fig. 5, and the datapath incorporates our proposed multiplier less correlator. The digitized signal is routed through get course programmable channelization for the purpose of isolating and isolating the LDACS channel from nearby DME beats. (T. H. Pham I. V., 2014) The correlator, a part of the beneficiary synchronizer, gets the twofold information from the picked channel and uses the sign cross connection strategy to attempt to gauge the image timing offset by perceiving the start of a ground-to-air outline. Different parts of the get channel baseband look like an OFDM recipient overall; the FFT module switches they got outline over completely to the recurrence space, which is in this manner balanced, demodulated, and decoded to create the genuine conveyed information. To guarantee solid and trustworthy gathering, the LDACS standard additionally prompts utilizing time-and recurrence area obstruction decrease techniques, as well as versatile evening out.

At the point when the station needs to communicate information, the mental rationale arranges the channelize to examine the LDACS RL transmission capacity and the range detecting chain is turned on. In this arrangement, the relate endeavours to distinguish the presence of a synchronization tile in the information got from the result of the channelize, and the data is then sent to the mental rationale.

Once a suitable channel is found, the communication chain is locked in place and mental logic sets up the RF module to include the selected channel for transmission. To create the LDACS structure, the baseband module uses QPSK refinement to map the information and applies IFFT to add a cyclic prefix. Before the sign is shipped off the D/A converter and RF modules, the ghostly covering channel transforms it to protect the demanding LDACS standard.

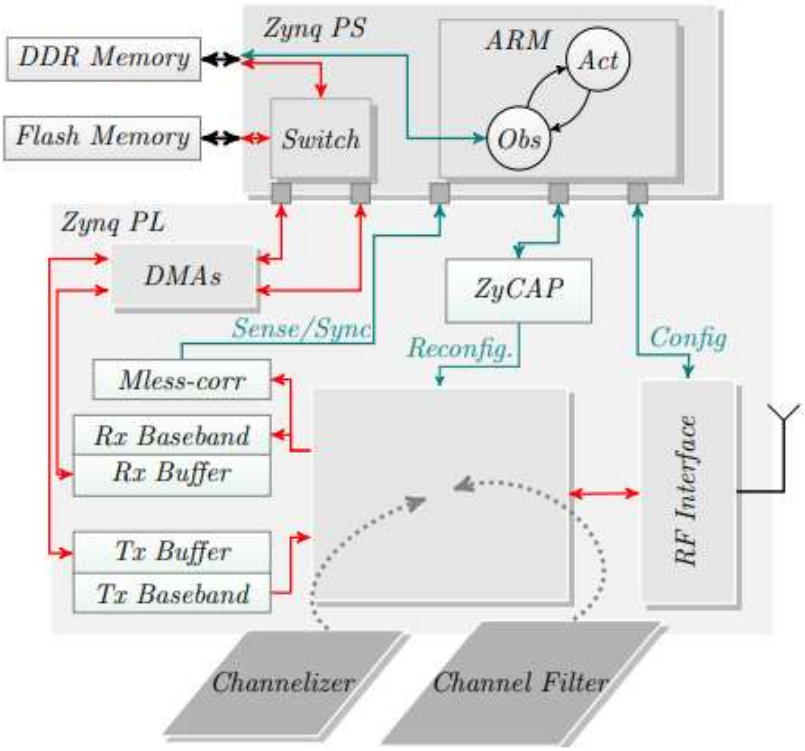


Figure 5: Integrating multiplier less correlator into the radio platform on Zynq

With mental justification, when a station needs to send information, channelization checks the LDACS RL send rate. Then the distance sensing chain kicks in. With this configuration, the correlator attempts to distinguish the presence of synchronous tiles in data obtained from channelling yields, and the data is sent to mental justification.

At the point when a reasonable channel is found, the send chain is locked in, and mental rationale then, at that point, sets up the RF modules to communicate utilizing the picked channel. To make the LDACS outline, the baseband modules apply the IFFT, embed the cyclic prefix, then, at that point, map the information utilizing QPSK balance. Preceding conveying the message to the RF and Computerized to Simple transformation modules, the otherworldly covering channel adjusts the sign to hold the demanding LDACS standard.

3.3 Integration into LDACS Radio Platform

The design of our radio stage for LDACS on a Xilinx Zynq chip is portrayed in a dense way in Fig. 6.

Tight association among programming and equipment handling blocks is made conceivable by the Zynq plan, which integrates a double centre ARM central processor with a programmable texture on a similar gadget.

The programmable rationale (PL) part of the Zynq executes the baseband usefulness (LDACS channelizes and channels) and associates with the radio wire with explicit points of interaction to speak with the mental programming exercises working on the ARM centre. Fast information move between the baseband modules and programming is made conceivable by committed direct memory access (DMA) regulators (or outside interfaces).

With parametric reconfiguration (for tweaking boundaries) and high velocity incomplete reconfiguration, which might be begun utilizing clear programming APIs, the stage conveys rapid powerful adaptability. To finish the RF front-end, a Simple Gadgets Promotion FMCOMMS4-EBZ board (in view of the AD9364) is associated with the receiving wire interface (see for more data on our LDACS radio stage).

The LDACS standard forces severe requirements on the beat state of the conveyed message and allows the exchange of data from the air to the ground across 23 channels. Thus, convoluted channels are utilized for beat melding during transmission and channelization during gathering. To diminish region overheads and power utilization, we execute this non-simultaneous capacity through fractional reconfiguration; the channelization module is stacked progressively during range recognition, while the channel module is stacked during genuine transmission.

By maximizing resource use, the PR method leaves enough resources available to build more complicated baseband modules, such as the correlator in this instance. As shown in Figure 6, the output of the channel filter or chandelier is connected (depending on the mode of operation) to a correlator module called Mlesscorr in a partially reconfigurable region (PRR). To reduce the multiplicative complexity, [6] replaced the filter bank-based spectral detection approach with an optimal channelization of LDACS and channel filters.

The correlator module peruses the channelize yield during a detecting activity and utilizations that data to decide whether a LDACS air-to-ground outline is being sent in the channel. Utilizing the channelize, four of these channels are simultaneously open, and under programming control, they are progressively taken care of into the correlator module. The mental programming deciphers the after-effects of detecting to pick the best transmission channel. The product sets a register bit in the correlator module so it could be used as a collector synchronizer for the OFDM demodulator stage during a normal get activity. Straightforward capability calls from the mental programming, for example, set baseband (spectrum sense), are utilized to do the parametric arrangement changes and the mode

progress through reconfiguration. Because of these capability calls, our system deals with every one of the low-level tasks expected to control the adjustment of boundaries or actual reconfiguration.

4. RESULTS

4.1 Implementation Results

We construct the suggested correlator separately on a Xilinx Zynq XC7Z045 FPGA in order to assess the resources it needs and calculate its power consumption. Table 2 displays the specific resource use of the multiplier less correlator's sub-modules. Utilizing the XC7Z045's moderate-grade texture, the plan accomplishes a functional recurrence of 190 MHz, and as it utilizes only 14% of the assets of the Zynq plan, the other baseband modules might be joined on similar equipment.

Sub nodel	FFs	LUTs	Slices	DSPs
Shift –add	312	190	75	1
Tap mux	1	6,452	2,444	1
Add-delay chain	25,845	26,789	6,479	1
Total utilisation (%)	25,000	30,912	8,156	1
% utilisation	6.9	15.6	15.3	1
Frequency	196 MHz			

Table 2: Detailed resource use of a solo module of a Zynq XC7Z045 device's multiplierless correlator.

For examination, we likewise made a multiplier-based correlator plan that was streamlined (in confinement, rendering direct structure), yet it must be executed on the greater XC7Z100 gadget (comparable design, yet offers more assets) due to the significant measure of DSP blocks required. (T. H. Pham S. A., 2013.) To improve speed with minimal measure of fine-grained asset usage, the advanced construction maps the defer parts using the inner pipeline registers inside the DSP block. Table 3 shows the results of the different executions. The

multiplier-based arrangement utilizes around 2% of the greater XC7Z100 gadget's LUTs and Goes back and forth (FFs) and 76% of its DSP blocks.

Our engineering is more qualified for on-board frameworks because of the multiplier less methodology's lower asset use, which likewise leaves an adequate number of assets accessible for the leftover baseband capabilities. These outcomes in a more minimal execution (and a more modest gadget with less static power utilization). The pipelined structure guarantees that the two plans have similar figure throughput (one result for every clock cycle) and dormancy (376 cycles), however multiplier-based correlators are more qualified for use in LDACS ground stations for overseeing and observing range designation across all airplane because of their higher working recurrence. Utilizing the Xilinx X Power Analyzer instrument, we also survey the plan's power use. The movement rates were delivered utilizing a post spot and-course recreation dump and genuine LDACS outline information as the contribution to the correlator for each clock cycle. At 125 MHz, the plan clock recurrence, the reproduction was run. The apparatus discovered that the multiplier less correlator consumed 1,160 MW altogether, of which 1,038 MW came from the correlator activity (dynamic power) on the XC7Z045 gadget. As indicated by the power investigation of the multiplier-based correlator running at a similar recurrence, the correlator contributed 3,166 MW of the complete unique power utilization. Thus, the recommended plan enjoys a 3 benefit in unique power utilization. The multiplier-based plan's more noteworthy gadget request likewise brings about an essentially higher in general power, highlighting the advantage of the proposed procedure.

Design	FFs	LUTs	Slices	DSPs	%Util	Fmax
Multiplier less	25,000	30,945	8,125	1	14.69(LUTs)	2015
Multiplier-based	12,986	2,569	2,365	1,600	75.35(DSP)	506

Table 3: Resources were compared between the multiplier-based correlator on the Zynq XC7Z100 device and the proposed correlator on the Zynq XC7Z045 device.

Lastly, using the XC7Z045 device, we assess the resource overheads of the design when it is included into our radio platform. Table 4 displays the outcomes of the implementation. Without taking into account the baseband modules that are not included here, it can be seen

that the suggested correlator provides roughly 65% of the system's overall LUT usage. Moreover, in the LDACS OFDM baseband, our correlator also serves as the receiver synchronizer, a crucial role necessary to enable proper decoding of the received data (over the critical LDACS ground to-air link). Our suggested correlator effectively cuts the resource usage by 16% compared to a standalone multiplier less cross-correlator that would otherwise need 9215 registers and 9574 LUTs more to help with receiver synchronization.

Under 26% of the gadget's assets are utilized by the general plan, leaving a lot of general (LUTs, FFs) and particular (DSP Blocks, BRAMs) assets accessible for baseband module execution and other register concentrated tasks for on-board LDACS frameworks.

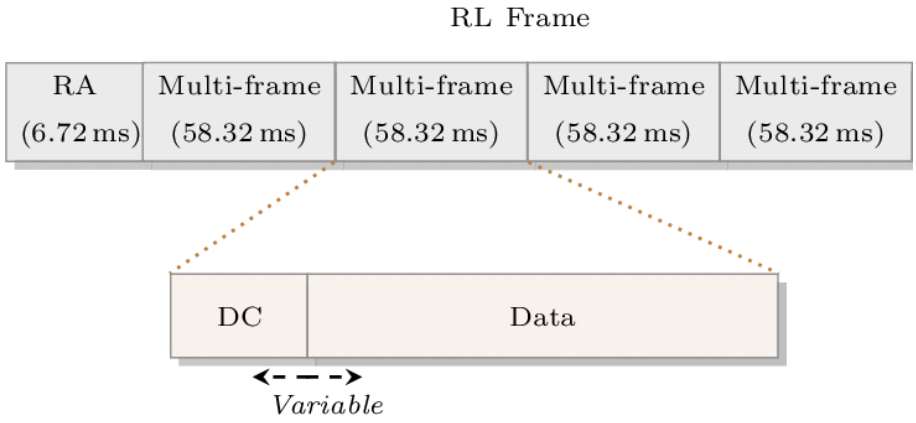
Sub-Module	FFs	LUTs	BRAMs(36/18)	DSPs
Channel Filter	2,441	2,452	0/1	25
Channelize	2,625	3,147	5/1	51
Mless-Corr	25,000	30,987	0	1
RF/IF	23,845	22,398	7/5	82
Recon fig	725	812	1/1	1
Total Utilisation	50,948	56,698	12/6	135
% utilisation	12,9	29.6	3.63	14.63

Table 4: Resource use of the suggested correlation into the Zynq radio platform

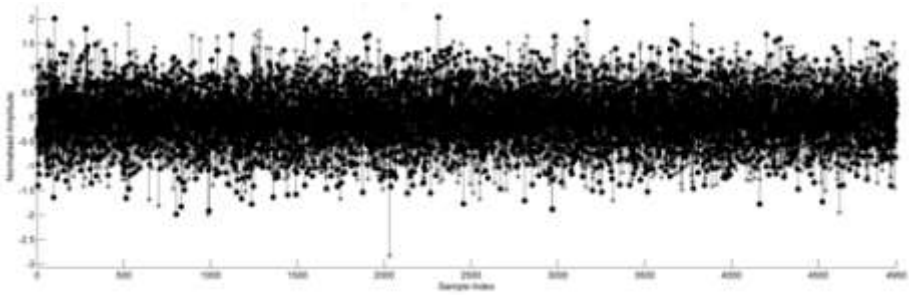
4.2 Spectrum Sensing Effectiveness

We make LDACS outlines in MATLAB and make AWGN parts to reproduce different got circumstances to test the productivity of the proposed correlator system in distinguishing the presence or nonattendance of transmissions under different SNR settings. We take on a solitary edge size (4950 examples) as the location window for both the multiplier-based and proposed correlator-based approaches. This casing size is in accordance with the stripped down RL outline that the standard proposes. In Fig. 6, the recurrence reaction plot for our test input outlines is shown; sub-plots 6a and 6b portray the genuine LDACS RL outline under zero clamour conditions and - 10 dB SNR conditions, individually. It tends to be shown that the clamour considerably affects the sent LDACS edge's recurrence reaction mark and commotion power level, which limits the utilization of clear energy discovery based

approaches. For such many conditions, a productive range detecting strategy ought to have the option to recognize the presence of LDACS transmission unequivocally.



A: Real, noise-free LDACS RL frame.



B: With -10 dB SNR, LDACS RL frame was received..

Figure 6: Plots of frequency for LDACS RL frames produced under various SNR settings.

These got outlines act as contributions for the equipment execution (as preloaded Slam contents), the MATLAB reproduction of the proposed multiplier-less correlator, and the multiplier-based model in our appraisal (in equipment). For equipment execution, the information sources are quantized to a 16-bit marked greatness fixed-accuracy design, and the MATLAB recreation model is assessed utilizing MATLAB's local exactness (twofold accuracy drifting point).

In Fig. 8, the result of the proposed correlator (equipment assessment) is introduced corresponding to got LDACS outlines under different commotion settings (SNR = 0dB, SNR = 10dB). The revelation of an impressive pinnacle (more prominent than 1.33 all others in the current casing) at test file 375, relating to the LDACS RL preface, lays out the presence of edge. The recommended correlator frequently gets solid tops at file 375, prompting positive

edge acknowledgment, despite the fact that the plots changed incredibly because of the different information commotion levels.

5. CONCLUSION

The steadily developing measure of data being moved among airplane and ground stations has demonstrated to be a lot for heritage aeronautical communication frameworks to deal with. (U. Epple, 2009) By giving extra channels to communication among air and ground stations and keeping up with concurrence with more seasoned L-band frameworks, new guidelines like LDACS plan to further develop air traffic the board. To give high information rate transmission to ensuing age worldwide ATM frameworks, L-DACS1 is being presented as an answer that can coincide with more established L-band frameworks. This study has described and assessed the hardware design of a brand-new synchronization technique for L-DAC1. The suggested approach is substantially more resistant to big CFO than the SOA method and is intended to achieve synchronization precision. Also, the suggested strategy may quickly and efficiently achieve strong synchronization throughout the prelude.

REFERENCES

1. *Action plan 17—Future communications study: Final conclusions and recommendations report," Eurocontrol/FAA/NASA, Tech. Rep. v1.1, Nov. 2007.*
2. *B. Kamali, "An overview of VHF civil radio network and the resolution of spectrum depletion," in Proc. Integr. Commun., Navigat., Surveill. Conf., May 2010, pp. F4-1–F4-8.*
3. *Challenges of growth 2008 summary report," Eurocontrol, Brussels, Belgium, Tech. Rep., 2008*
4. *Diaz et al., "A new approach to sign-bit-based parameter estimation in OFDM receivers," Circuits, Syst., Signal Process., vol. 34, no. 11, pp. 3631–3660, 2015.*
5. *F. Kastensmidt and P. Rech, "Radiation effects and fault tolerance techniques for FPGAs and GPUs," in FPGAs and Parallel Architectures for Aerospace Applications. Cham, Switzerland: Springer, 2016, pp. 3–17.*
6. *F. Shamani, R. Airoldi, T. Ahonen, and J. Nurmi, "FPGA implementation of a flexible synchronizer for cognitive radio applications," in Proc. Conf. Design Archit. Signal Image Process., Oct. 2014, pp. 1–8.*

7. *F. Shamani, R. Airoldi, V. F. Sevom, T. Ahonen, and J. Nurmi, "FPGA implementation issues of a flexible synchronizer suitable for NC-OFDMbased cognitive radios," J. Syst. Archit., vol. 76, pp. 102–116, May 2017.*
8. *J. S. Park and T. Ogunfunmi, "Efficient FPGA-Based Implementations of MIMO-OFDM Physical Layer," Circuits, Syst., Signal Process., vol. 31, no. 4, pp. 1487–1511, 2012.*
9. *L. Hanzo and T. Keller, OFDM and MC-CDMA: A Primer. New York, NY, USA: Wiley, 2006.*
10. *M. Sajatovic, B. Haindl, U. Epple, and T. Gräupl, "Updated LDACS1 system specification," SESAR Joint Undertaking, Brussels, Belgium, Tech. Rep. EWA04-1-T2-D1, 2011.*
11. *N. Lashkarian and S. Kiaei, "Class of cyclic-based estimators for frequency-offset estimation of OFDM systems," IEEE Trans. Commun., vol. 48, no. 12, pp. 2139–2149, Dec. 200*
12. *T. H. Pham, A. P. Vinod, and A. S. Madhukumar, "An efficient dataaided synchronization in L-DACS1 for aeronautical communications," in Proc. ACM Int. Conf. Data Mining, Commun. Inf. Technol. (DMCIT), 2017, pp. 21:1–21:5.*
13. *T. H. Pham, I. V. McLoughlin, and S. A. Fahmy, "Robust and efficient OFDM synchronization for FPGA-based radios," Circuits, Syst., Signal Process., vol. 33, no. 8, pp. 2475–2493, Aug. 2014.*
14. *T. H. Pham, S. A. Fahmy, and I. V. McLoughlin, "Low-power correlation for IEEE 802.16 OFDM synchronization on FPGA," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 21, no. 8, pp. 1549–1553, Aug. 2013.*
15. *U. Epple, S. Brandes, S. Gligorevic, and M. Schnell, "Receiver optimization for L-DACS1," in Proc. IEEE/AIAA 28th Digit. Avionics Syst. Conf., Oct. 2009, pp. 4.B.1-1–4.B.1-12.*