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Efficient High-Speed Multiplication with Modified Vedic Multiplier using Modified HSCG-SCG Adder in Verilog HDL

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Abstract

The Modified Vedic Multiplier is a multiplication algorithm inspired by ancient Vedic Mathematics principles, employing a unique approach involving vertical and crosswise calculations. This research introduces the Modified HSCG-SCG Adder, an improved version of traditional binary adders, which employs a decoder to generate partial products and a carry tree to compute the final result. The synergy between the Modified Vedic Multiplier and the Modified HSCG-SCG Adder offers notable advantages over conventional multiplication methods, including reduced latency, lower power consumption, and increased processing speed. This combination is particularly well-suited for applications requiring high-speed multiplication, such as digital signal processing, image processing, and cryptography. The implementation of this algorithm is achieved through Verilog Hardware Description Language (HDL), enabling simulation and testing using hardware simulators like Vivado.

Keywords: Adders, HSCG-SCG Adder, Multipliers, Vedic Multipliers, Verilog HDL, High-Speed Multiplication, Power Efficiency, Digital Signal Processing, Vivado.

1. Introduction

Binary multipliers are a widely used building block element in the design of microprocessors and embedded systems, and therefore, they are an important target for implementation optimization. Current implementations of binary multiplication follow the steps of Recoding of the multiplier in digits in a certain number system.Digit multiplication of each digit by the multiplicand, resulting in a certain number of partial products, Reduction of the partial product array to two operands using multi operand addition techniques, carry-propagate addition of the two operands to obtain the final result. The recoding type is a key issue, since it determines the number of partial products. The usual recoding process recodes a binary operand into a signed-digit operand with digits in a minimally redundant digit set. Specifically, for radix-r (r = 2m), the binary operand is composed of non-redundant radix-r digits (by just making groups of m bits), and these are recoded from the set {0, 1,,r − 1} to the set {−r/2,..., −1, 0, 1, . . ., r/2} to reduce the complexity of digit multiplications. For n-bit operands, a total of n/m partial products are generated for two‘s complement representation, and (n + 1)/m for unsigned representation. Radix-4 modified Booth is a widely used recoding method, that recodes a binary operand into radix-4 signed digits in the set {−2, −1, 0, 1, 2}. This is a popular recoding since the digit multiplication step to generate the partial products only requires simple shifts and complementation. The resulting number of partial products is about n/2. Higher radix signed recoding is less popular because the generation of the partial products requires odd multiples of the multiplicand which cannot be achieved by means of simple shifts but require carry- propagate additions. For instance, for radix-4signed digit recoding. The digit set is {−8,−7,..., 0,..., 7, 8}, so that some odd multiples of the multiplicand have to be generated. Specifically, it is required to generate ×3, ×5, and ×7 multiples. The generation of each of these odd multiplies requires a two-term addition or subtraction, yielding a total of three carry-propagate additions.

The motivation behind the design and implementation of the Modified Vedic Multiplier Using Modified HSCG-SCG Adder is to improve the speed and efficiency of binary multiplication

operations in digital circuits. Multiplication is a fundamental operation in many digital circuits, including microprocessors, digital signal processors, and graphics processing units. Therefore, improving the performance of the multiplier circuit can have significant benefits in terms of overall system performance and power consumption. The Vedic Multiplier is a type of multiplier circuit that is based on the ancient Indian Vedic mathematics. It uses a set of sutras or aphorisms to simplify the multiplication operation and reduce the number of partial products that need to be added to obtain the final result. The Vedic Multiplier has been shown to be faster and more efficient than other types of multipliers, such as the array multiplier and the Booth multiplier.

The HSCG-SCG Adder is a type of adder that is faster and more efficient than other types of adders, such as the ripple carry adder and the carry look ahead adder. It uses a decoder to generate the possible combinations of sum and carry bits for the addition of two binary numbers. By combining the Vedic Multiplier with the HSCG-SCG Adder, the design and implementation of the Modified Vedic Multiplier Using Modified HSCG-SCG Adder aims to create a faster and more efficient multiplier circuit. The modified design of the Vedic Multiplier and the HSCG-SCG Adder takes advantage of the strengths of both circuits to reduce the overall delay and power consumption of the multiplication operation. The modified design also simplifies the implementation of the circuit and reduces the number of logic gates required. This can lead to improved system performance, reduced power consumption, and lower manufacturing costs.

2. Literature Survey

Kumari, A., Kharwar, S., Singh, S., Mohammed, M.K.A., Zaki, S.M. (2023) [1] presented model consists of slice LUT‘s and power of the proposed 2 × 2 and 4 × 4 novel decoder based Vedic multiplier using Urdhva Tiryakbhayam sutra were calculated and compared with conventional multiplier. Therefore, utilizing the advantages of Vedic architectures with the proposed idea to solve the problem of balancing power consumption and speed increased in circuits. Patel, Chiranjit R., et al (2020)[2]. Paper proposes the design and implementation of an enhanced binary multiplication technique.. The main objective of this paper is to design an improved binary multiplier which is faster and low-powered. Dhanasekar, S., et al(2022)[3]. optimized area for a 64-point FFT processor using a Vedic multiplier with a modified compressor adder has been proposed. Multi-radix Akhter, Shamim., et.al(2019)[4], presents a modified binary multiplier using Vedic mathematics. The paper proposes a modification in the previously published Vedic multiplier circuit. The suggested modified Vedic multiplication technique is more efficient in terms of delay and area. The proposed circuit is implemented in VHDL. The Mentor Graphics ModelSim tool is used for HDL simulation, and the Xilinx ISE Design Suite 14.1 is used for circuit synthesis. The simulation is done for 4-bit, 8-bit, and 16-bit multiplication operations. In this paper, the simulation waveforms are shown only for 4-bit multiplication operation based on the modified Vedic multiplication technique.

Kumar, Prashant,and Sangeeta Singh (2019) [5],proposed design demonstrates significant improvements in circuit complexity, area efficiency, and quantum cost while retaining performance in terms of latency and area usage. Coplanar crossovers are properly realized using 180° clock zones. Murugesh,M.Bala,et.al(2020)[6].paper presents a modified binary multiplier using Vedic mathematics. The paper proposes a modification in the previously published Vedic multiplier circuit. Praveen Kumar, Y. G., et al(2022)[7] primitive constraints in any VLSI system design are power, delay and area. Systems based on CMOS logic consume more power and area. Higher power dissipation will have a direct effect on the lifetime and performance of digital systems. Adders and multipliers form the core of almost all the digital systems like Microprocessor, Digital Signal Processors (DSPs), etc., so the adders and multipliers need to be optimized in terms of power, area

and delay for an efficient and cost-effective processor design. Padmavathy, T. V., S. Saravanan, and M. N. Vimalkumar.,et.al(2022)[8]. design of adder plays a major role in deciding overall performance of system as it is a major building block through generations of design in an innovative design of circuits. In VLSI system and signal processing field applications, various versions of adders are utilized. In applications of signal processing, in recent days, major role is contributed by Finite Impulse Response (FIR) filter Rakesh, S., and KS Vijula Grace et.al(2022)[9]. paper presents different power efficient multiply accumulate architectures based on modified parallel prefix adders. A general multiply accumulate unit consists of a multiplier, an adder and an accumulator. The multiplier used in this study is a Vedic multiplier and the parallel prefix adders that are brought into this research include Kogge Stone adder, Brent Kung adder, Han Carlson adder and Hybrid Han Carlson adder. The pre-processing and post-processing stages in those adders which mainly consists of exclusive OR operations are modified using a switch level model of the exclusive OR gate. The corresponding modified adder is also used in the Vedic multiplier for adding the partial products. The performance analysis of the different multiply accumulate models is done in terms of power and figure of merit.

Padma, C., P. Jagadamba, and P. Ramana Reddy et.al(2021)[9]. . paper presents a modified binary floating-point multiplier using Vedic mathematics and a modification in the previously published Vedic multiplier circuit has been proposed. Pasuluri, Bindu Swetha, and VJK Kishor Sonti et.al(2021)[10]. . In this article, we propose a first order analogue LPF based on a simple current mirror Operational Transconductance Amplifier (OTA), as well as a digitized LPF with Vedic multipliers for bio-medical applications. The analogue filter is intended for use in ECG signal acquisition, and then it works in the weak inversion area with extremely low power consumption. The current mirror-based OTA employed here streamlines the entire design of the OTA as well as lowers the number of available components required to implement the filter. The filter was created and modelled on 45nm CMOS technology. Additionally, this article represents a major advancement in the implementation of a FIR filter based on the updated Nikhilam Sutra Multiplier.Choudhary, Kuldeep, et al (2022)[10]. We live in a digital world surrounded by digital content in the form of images, videos, and much more which consume extensive power. With the extensive use of digital content in portable gadgets power consumption has been critical issue to act upon. The multiplier is the core component used in image processors and digital signal processors and by altering the properties of the multiplier system provides superior performance.Sravana, J., et al2 (2022)[11]. This paper demonstrates the improved adaptation of the Vedic Multiplier using the Vedic standards, which includes old sutras. In this paper, current and proposed model are examined. Verilog HDL is utilized to execute the improved adaptation of Vedic Multiplier. Streamlined proposed model can likewise be utilized to achieve higher-request bits duplication exercises up to 32 bits. Vedic Multiplier up to 32-bit, the reproduction results are examined. These outcomes showed that the streamlined Vedic multiplier changed the execution improvement measurements, for example, time delay, also in device use too. Alongside this, a correlation is made among existing and enhanced proposed model to recognize about the presentation improvement measurements.

3. Proposed Methodology

In economics, a multiplier refers to the effect that a change in one economic variable has on another variable. For example, the government spending multiplier refers to the increase in overall economic output that results from an increase in government spending. Similarly, the investment multiplier refers to the increase in overall economic output that results from an increase in private sector investment. The size of the multiplier depends on various factors, such as the type of spending or

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investment and the state of the economy. The HSCG-SCG adders are a type of adder that use a decoder to generate partial sums, which are then combined to produce the final sum. They are known for their low power consumption and are often used in low-power applications. Combining modified Vedic multipliers with HSCG-SCG adders is an area of research that aims to develop more efficient arithmetic units for digital signal processing and other applications. A HSCG-SCG Adder is a type of digital circuit that is used to add two binary numbers. The circuit is based on a decoder, which is a combinational logic circuit that converts an n- bit input into 2^n outputs. In a HSCG-SCG adder, the decoder is used to generate the sum and carry bits of the addition operation. The basic principle of a HSCG-SCG Adder is to use a decoder to generate the possible combinations of sum and carry bits for the addition of two binary numbers. The input bits are fed into the decoder, which generates the sum and carry bits based on the input combination. The generated sum and carry bits are then combined to obtain the final result. The advantage of a HSCG-SCG Adder is that it is faster and more efficient than other types of adders, such as the ripple carry adder, or the carry look ahead adder. It has a lower delay and requires fewer logic gates, which results in lower power consumption and area. However, the disadvantage of a HSCG-SCG Adder is that it requires a large decoder circuit, which can be complex and difficult to design. HSCG-SCG adders are often used in high-speed digital circuits, such as microprocessors, digital signal processors, and graphics processing units. They are also used in arithmetic logic units (ALUs), which are the fundamental building blocks of digital processors.

3.1 Working

The motivation behind the design and implementation of the Modified Vedic Multiplier Using Modified HSCG-SCG Adder is to improve the speed and efficiency of binary multiplication operations in digital circuits. Multiplication is a fundamental operation in many digital circuits, including microprocessors, digital signal processors, and graphics processing units. Therefore, improving the performance of the multiplier circuit can have significant benefits in terms of overall system performance and power consumption. The Vedic Multiplier is a type of multiplier circuit that is based on the ancient Indian Vedic mathematics. It uses a set of sutras or aphorisms to simplify the multiplication operation and reduce the number of partial products that need to be added to obtain the final result. The Vedic Multiplier has been shown to be faster and more efficient than other types of multipliers, such as the array multiplier and the Booth multiplier. The HSCG-SCG Adder is a type of adder that is faster and more efficient than other types of adders, such as the ripple carry adder and the carry lookahead adder. It uses a decoder to generate the possible combinations of sum and carry bits for the addition of two binary numbers. By combining the Vedic Multiplier with the HSCG-SCG Adder, the design and implementation of the Modified Vedic Multiplier Using Modified HSCG-SCG Adder aims to create a faster and more efficient multiplier circuit. The modified design of the Vedic Multiplier and the HSCG-SCG Adder takes advantage of the strengths of both circuits to reduce the overall delay and power consumption of the multiplication operation. The modified design also simplifies the implementation of the circuit and reduces the number of logic gates required. This can lead to improved system performance, reduced power consumption, and lower manufacturing costs.

3.2 CSLA using HSCG-SCG adder.

The present generation chips consist of various types of adders such as CSLA, RCA, carry bypass adder, carry look ahead adder and still many more. But this addition requires huge resources such as LUTs and PLBs, which causes to increase the power, delay consumption. To overcome these drawbacks, the proposed HSCG-SCG-CSLA will be effectively used in ALUs. As per this addition process the proposed structure is modified from SQRT based CSLA. And from SQRT based CSLA RCA-BEC based structure will be modified with HSG, HCG, FSG and FCG units. For implementing

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these building blocks, in this paper new XOR gate is developed with reduced gate count thus quantum cost also reduces. Generally, the XOR gate consists of two NOT gates, two AND gates and one OR gate in its logic realization. The proposed XOR gate is realized as shown in Figure 1, while it consists of two AND gates, one OR gate and one NOT gate. By modifying the gate level structure, its logical operation is justified as original XOR function with optimized Quantum Cost.

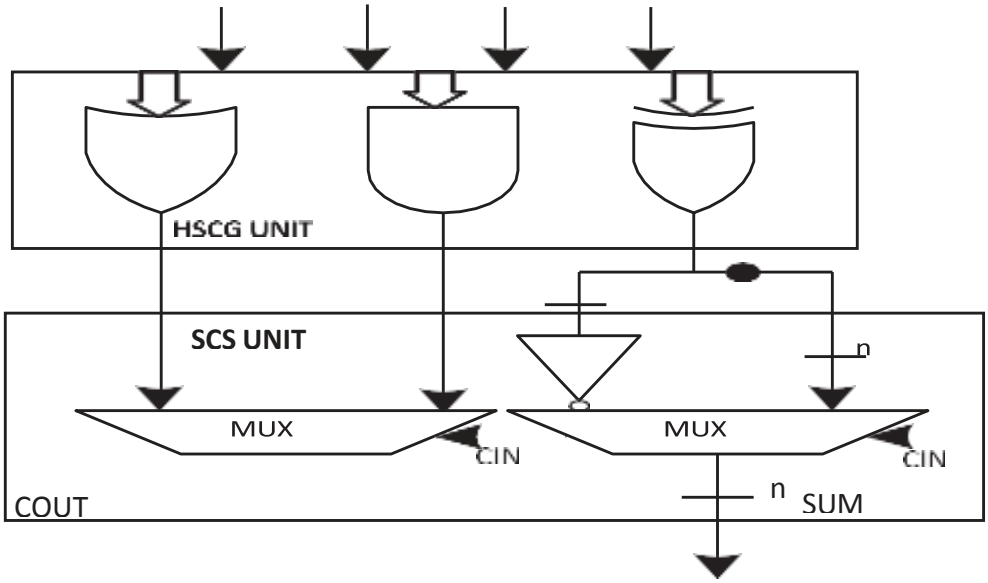

Figure 1. Block Diagram for HSCG - SCG Adder

The HSG block is defined by the generation of sum for forward stages, even though it is having both half adder-based sum and carry generation. The HCG is defined by the generation of carry for forward stages. Similarly, the FSG is used to generate the final sum using switching operations. Whereas, FCG unit generates the Final carry with low path delays. The sum of the HSG unit is generated by the proposed XOR gate, which allows the design to reduce the power dissipation. From the HSG unit half of the Sum is generated using proposed XOR gate. Carry of HSG unit and another half carry from HCG blocks are applied to the FCG units for final carry generation; hence the path delays will reduce. The combined operation of HSG and HCG blocks creates the HSCG block, similarly SCG block created by parallel operation of FSG and FCG blocks.

In the FCG, multiplexer selection gets the input from Cin. If Cin = 0, then sum operation generates based on the non-inverting form of XOR gate from HSG block, and carry operation generates based on the AND output from HCG block. if Cin = 1, the multiplexer switches the inputs, the sum operation generates based on the inverting form of XOR output from HSG block, and carry operation connects the input from OR gate output. In the proposed design, redundant logic functions of each group structure have been identified for reducing complexity and gate count of adder circuit. The main goal of this proposed work is to design the adder based on SQRT-CSLA circuit with the help of HSCG-SCG-FA alone instead of using a combination of both HA, FA and BEC units. The N-bit HSCG-SCG-CSLA adder is spitted into $\sqrt{N}$ + 1 groups, and each group is operated in parallel manner to give the fastest outcomes as shown in figure 3 and figure 4.Generally, irrespective of bit length, RCA will be presented to adjust the bit lengths. Each group consists of multiple number of HSCG-SCG-FAs based on their input bit width.

Figure 2 represents the 16-bit HSCG–SCG-CSLA block diagram which contains the 5 stages such as ($\sqrt{16}$ + 1). The input bit length for each group is incremented order with respect to the group size. Every group has two major inputs namely A and B, other than carry input. Here, the bit length of each

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group varies chronologically with respect to its group size. For an instance, group 2 has the 2-bit width for *A*and *B* inputs positioned from [3:2] each, group 6 has the 6-bit width for *A* and *B* inputs positioned from [21:16] each. Each group is connected in ripple carry propagation manner, thus the carry out from the one group is applied as the input to the next group.From the basis of figure 3, the *N*-bit HSCG–SCG-CSLA is developed with group *M* stages as shown inFigure 4, so it can be used for 8-bit,16-bit, 32 bit and 64-bit implementations, respectively and the major use of this proposed adder is thatit can be used as reconfigurable purpose. Generally, in signal processing domain and in arithmetic operations, the input variables sizes are changes continuously; in those situations, the reconfigurable adder is required. By changing the parameter of *N*, the length of the adder changes according to the user requirement.

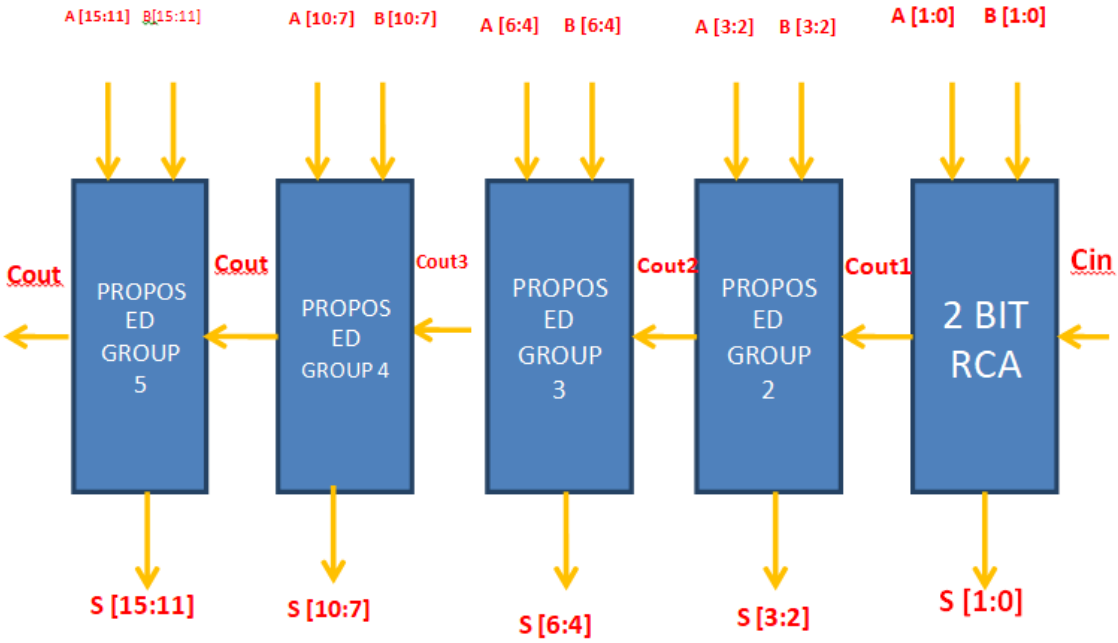

Figure 2. Block diagram of proposed 16-bit HSCG–SCG CSLA.

3.3 Modified Vedic multiplier

In the proposed work, the two parallel adders are replaced by of HSCG-SCG-CSLA for the better execution of the multiplier architecture. The recommended modified Vedic multiplication methodology is done in the following for 4 bit inputs, A(A3 -A0) and B(B3 -B0) and 8 bit output S (S7 -S0).A multiplier of 2 bit is used to calculate intermediate stage results, and the output is 4 bits. (A3A2) (B3B2) using 2 bit multiplier generates result: S33S32S31S30 (A3A2)(B1B0) using 2 bit multiplier generates result: S23S22S21S20 (A1A0)(B3B2) using 2 bit multiplier generates result: S13S12S11S10 (A1A0)(B1B0) using 2 bit multiplier generates result: S03S02S01S00. The 4-bit of HSCG-SCG-CSLA is used to add three 4 bit data inputs: S23S22S21S20, S13S12S11S10 and S31S30 S03 S02. The proposed 4-bit modified Vedic multiplier is designed and the Fig. 2 shows it. The last two MSBs of HSCG-SCG-CSLA outputs are given as inputs to OR gate. In addition, the last stage 4-bit RCA is replaced by 2 bit adder circuit through which the output value of OR gate can be controlled. One of the inputs to last stage 2-bit adder is obtaining from the output of or gate. Similarly, a 4 bit of HSCG- SCG-CSLA block is a must needed for 8 bit Vedic multiplication design. Figure 3, shows 32- bit modified Vedic multiplier.

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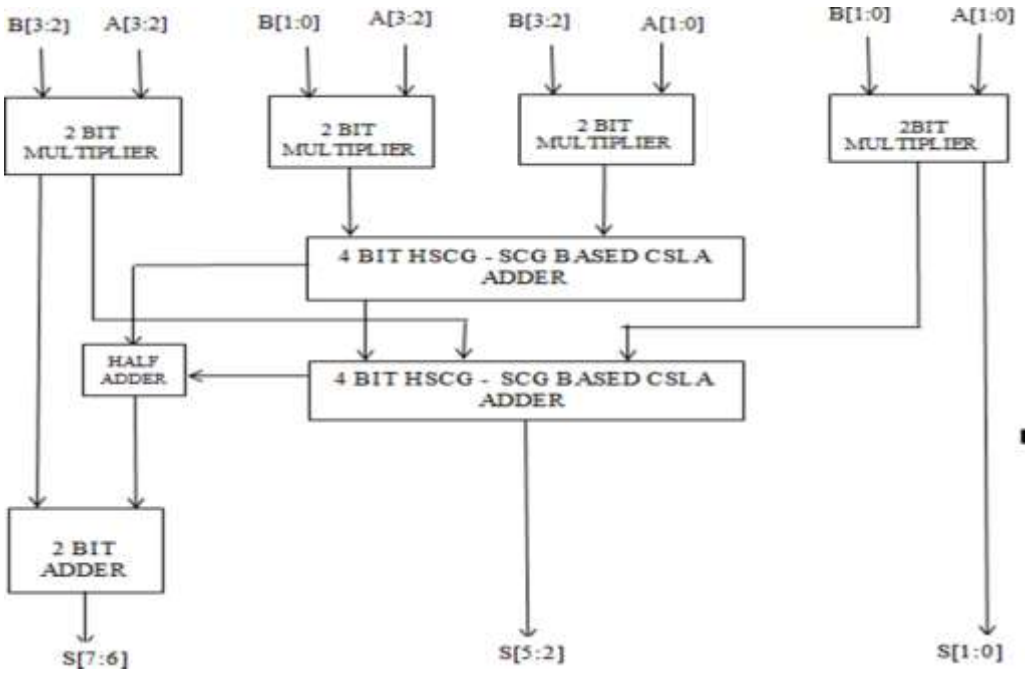

Figure 3. Modified 4 Bit Vedic Multiplier

4. Results and discussion

The simulation results will done by using in Vivado ISE.The timing, power and synthesis reports listed below

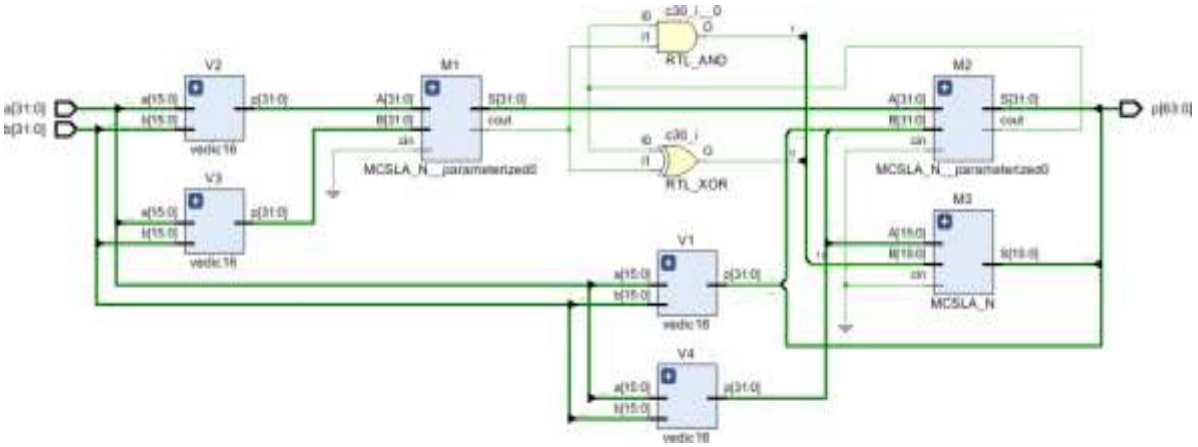

Figure 4. 64 Bit Proposed Vedic Multiplier RTL Schematic

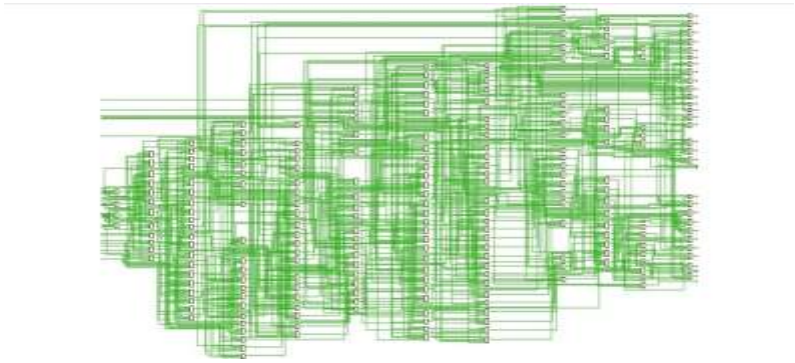

Figure 5. 64 Bit Proposed Vedic Multiplier Synthesized Design.

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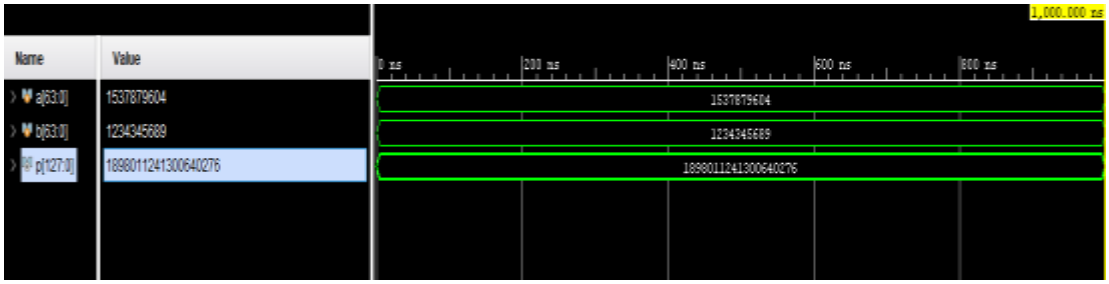

Figure 6. 64 Bit Proposed Vedic Multiplier Simulation Result:

Table: 1 Comparison of 32-bit Vedic multipliers

Multiplier Type	LUT's	Slice Registers	Bonded IOB's	Dynamic Power (W)	Total Power(W)	Delay (ns)
Existing Decoder Based Vedic Multiplier	8311	2397	256	448.824	450.498	3.6635
Proposed HSCG_SCG Based Vedic Multiplier	8147	2424	256	448.451	450.125	2.0371

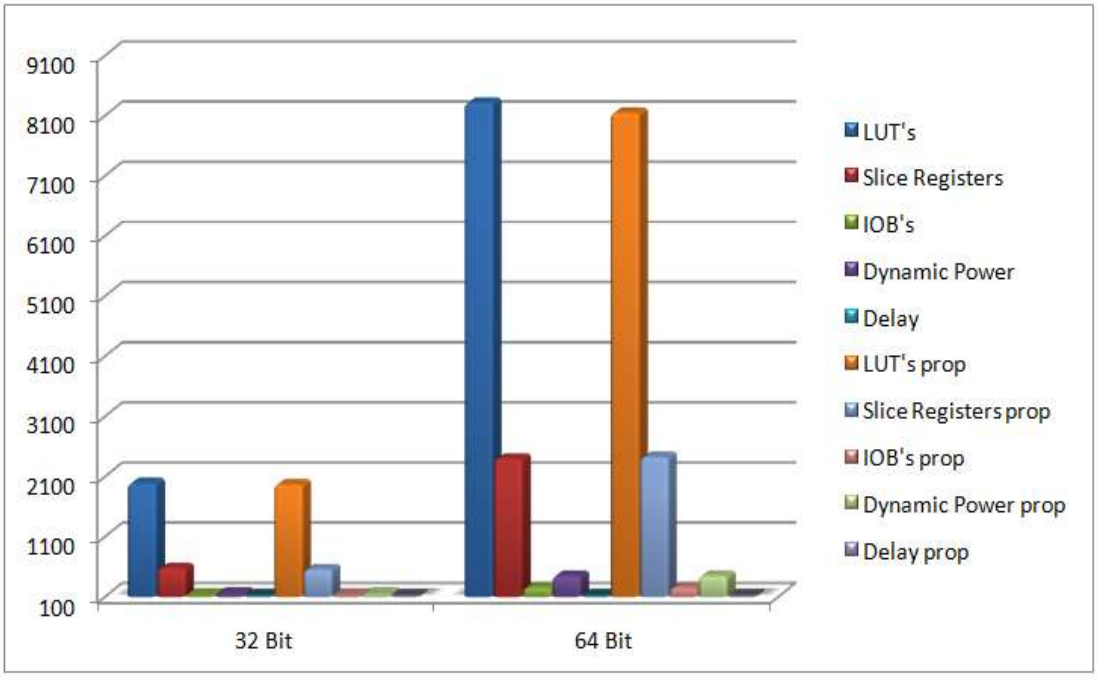

Figure 7. Comparisons for 32- Bit and 64-Bit Vedic Multipliers

5. Conclusion

This work has presented a systematic method for binary multiplier circuits which is based on Vedic mathematics. When it comes to the terms of time delay then the proposed system is more efficient

than existing methods. Elongation for a higher bit size can be done with help of proposed technique. Moreover, adders of different architectures can be used in the HSCG-SCG-CSLA design used in the proposed modified Vedic multiplier. Among many techniques modified architecture is used to increase and speed up the multiplication

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