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LOW-POWER ADC WITH TRANSVERSE READ TECHNIQUES USING SPINTRONIC RACETRACKMEMORY DEVICE

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ABSTRACT: In this paper a low power analog to digital converter using transverse read technique using spintronic racetrack memory is proposed.The efficiency in energy is promised by Domain Wall (DW) motion in analog computations, which are done by using magnetic wires are called nano wires that induces current in a spintronic racetrack memory. Analog to digital converter's feasibility explored in this paper depending on current induced motion in domain wall motion and introduces a Analog to Digital Converter (ADC) using racetrack magnetic nano wires by using transverse read techniques. DM memory, is an extension to STT-MRAM (SpinTransfer Torque-Magnetic Random Access Memory),which stores multiple bits, every bit is in an separate domain innanowire. By using orthogonal access point to nano wire is carries DWM access mechanism just like conventional MJT (Magneto-Tunnel Junction) of STTMRAM.The place where dense ADC array is needed, this racetrack ADC is applicable, for example image sensors.

KEY WORDS: Racetrack memory, Analog to digital converter, Domain wall(DW), (STT-MRAM)spin transfer torque-magnetic random access memory.

I. INTRODUCTION

And also in very high speed massive parallel sensors like imagers, every photodiode comprise of compact ADC for parallel conversion and moderate accuracy.

Conversion of that data faces challenges if CMOS implementations are used. Mainly there are two challenges. Most difficult and first challenge tedious thing is that integrating of ADC's with each and every channel or pixel since analog circuits have large area. This is highlighted by poor analog circuit scaling in CMOS because advanced technologies have various process variations. Second one is that ADC's higher static power.To balance the performance and area/power, most of image sensors with high speed uses image sensors in sensor arrays in column parallel ADC's.Though, image sensors having high frame rate are needed for emerging applications, images like time-of-flight, vision in integralmachine,3-D HD television imaging [2].

In recent times, many numbers of novel materials and devices have proposed in order to reinstate MOS transistors for particular applications. The Current induced DW motion is discovered which leads to inventions of many spintronic devices those provides promise for high endurance, low power, nonvolatility and high density[3]. With PMA (Perpendicular Magnetic Anisotropy) in MgO/CoFeB structures,

many magnetic domains which are separated by Domain Walls for multi bit memory (nonvolatile) can be managed in single nanowire.To propose a logic computation, mcell device which has four-terminals uses DW switching.It is reported that DW neurons are suitable for comparing current operations and also works as current comparators like SAR ADC. Though, Domain Wall neuron ADC not shown much influence on spintronic devices in many areas (even DAC) are still uses CMOS to implement [4].

Memories based on charge are replaced potentially by spintronic memories. Charge based memory is suffered with higher power leakage consumption. Specially, DWMs, sometimes taken as "Racetrack" memories,that provides higher density (i.e., greater than STT-MRAM) and same access time and powercompared to remainingother memories [5]. The above characteristics help DWM an exhilarating potential for replacement of caches based on SRAM. Nano wires are basic parts in Spintronic DWMs. These are used to build them. Here every nano wire comprises of domains and these separated by DWs.Access mechanism is the main concern about DWM technology. Shifting mechanism is required to access data and desired domain must needed as per the alignment of access port, all this is because of DW nano wire can able to store multiple bit.While shifting additional "padding" domains are needed on each and every side to the datadomains in order to avoidloss of data. To reduce and accelerate energy which compared to other current based, shift-based writing is proposed.Fixed domains of polarization opposing in plane was present in the port of read/write, but which is orthogonal to nanowire, permit a particularpolarization which is to be shifted into domain that is aligned [6].

However, the process of accessing data is similar to STT-MRAM which has mechanisms with lower power. The mean of energy will increase by shifting data back and forth significantly [7]. As result it leads tosignificant effort that improves data placement in designing techniques and it minimizes the shifting. This must take considerablyconcern.Even though shifting technique is minimized and it concerns dynamic energy of DWM. Furthermore, by technology scaling the interest over improved density in memory leads to continues the trend memory structures ultra minimization. Due to this type of fashion in scaling will leads to introduce many new and additional faults in fabrication imperfection that may also leads to number of faults and irregularities in DWM along with memory alignment and also some pinning faults during shifting [8].So, approaching of fault tolerance isvery critical to make Domain wall memory commercially viable and technology mature.

II.LITERATURE SURVEY

A racetrack memory is a device nothing but magnetic nanowire comprise of multiple magnetic domains and are separated by Domain Wall.At a particular assigned position a DW magnetic strip is placed within it and a local spin polarity stores a single bit data in it.With the help of induced horizontal current generally a DW can shifted along strips of magnet. Generally, aPositive Mental Attitude(PMA)racetrack structure memory which comprise of single magnetic nanowire and write and read ports are two MTJs present in it.Current pulse is given to Iwrite which is write port in the MTJ, magnetic domain which is present in magnetic nano wire beneath the MTJ nucleated via spin transfer torque [9].

During that period of time, Ishift which is a horizontal current can pass some data along

with magnetic stripe. By asserting simultaneously write and shift currents, by this DWs sequence can be stored by racetrack.This work has explorespotentials of building many hundreds of DWs in single nanowire. Having such higher density, then efficiency of area can be higher than 1 F2/bit, giving higher density than many other technologies of nonvolatile memory [10]. The magnetic domains polarization which is under the read port of MTJ and it is detected by resistance sensing, that was affected via tunnel magneto resistance effect. The speed of reading access of MTJ is reported as 4 ns,array megabyte-scale.Furthermore, these devices implements over CMOS transistors which reduces interconnection delay and total area in backend process.

The electron scattering that dependent on spin can cause current via magnetic nanowire to be in spin polarized. If an electron which is spins polarized crosses a DW, then its polarization rotates 180^0 and it also changes from one domain to another. In order to maintain overall momentum of spin angle, the current charge is transferred to local magnetization in spin polarization and creates spin torque and which leads to the movement of DW.DW moves in against the direction to current charge that is along with spin-polarized electrons.Both experimental and theoretical studies clearly show that threshold of current charge density for the motion of DW in PMA nanowire based on cross sectional area of nano wire. As per adiabatic spin transfer torque modelthe density of threshold current decreases along with reductionin thickness and width [11].DW moves with nano wire, if and only if driving current is greater than threshold current.High velocity of DW motion can generate by high driving current.

The TR helps in determining the number of ‘ones’ in data which is stored by calculating the point of end-to-access magnetoresistances of a nanowire. Anisotropic Magneto Resistance (AMR) of the nano wire generates resistances due to walls magnetic orientation and domain walls.Using Tunneling Magneto Resistance (TMR) the novelty in work will be distinguished by capturing phenomena of number of different states having ‘1’. It is having a nano wire on read head is very identical to the Multi-Level Cell Based Magnetic Tunnel Junction (MLC-MTJ).The main advantage over MLCMTJisthat dipolar coupling is absent in between both two domains. The interactions between exchange energies and anisotropy in a nanowire found in two basic categories of wall: The first one is transverse. This category has reflection symmetry which is across a line i.e., perpendicular to vortex and magnetization,where rotation of magnetization is across the DM [12]. The domain motion which is across the vortex walls ismuch slower and it also needs high currents than the transverse walls. So, the DWM having transverse walls are taken in computing and storage applications. Note this point that “transverse” wall would not confused with “transverse” read.

Falicov and Cabrera theoretically discovered that variations in magnetic network resistance will be outcome of backscattering of electronsat DWs because of the mismatch in between the magnetic moment and electron spins. Two mechanisms are taken into consideration: one is paramagnetic: electrons reflected from thewall and second one isDiamagnetic: electron force travels in between unmatched domains.With the help of this theory, Berger et. al [13] calculatedtensor resistivity of a network that contains domain walls and this approach isrestricted to classical Boltzmann

approximation,the main and important, considered onlysingle-dimensional flow of current,and it was system with insufficient approximation.Furthermore, spin transport via the walls is not well-established by then; so, their estimation lacks idea of accumulation of spin in the wall. After, Tatara et al. [14] extended the present study in order to address the limitation, 3-D current depends on linear response theory. Gregg et al. [15] suggested a contrasting theory which mis-tracks, magnetic orientation of wall is tracked by electron spin, is underlaywitha reason behind electron scattering. This is the theorywhich leads to giant evolution.

The proposed method of forced lector stack technique can be implemented with the supply voltage of sub-threshold Voltage for designing CMOS gates in order to reduce the leakage current in active mode and standby mode [16].

III. LOW POWER RACETRACK ADC

Many of spintronic devices have beenappropriate for the computations in current-modedue to their characteristics directly involved with mathematicalrelationship of current. Most of operations of mLogic,DW neuron and all-spin-logicare alldepends on only current.

Proposed converter using racetrack is totallycompatible with allspintronic logic devices works incurrent-mode.By using and combining with all these different approaches, mixed signal current-steering morecomplex systems can be implemented.Although, most of CMOS modules still works as voltage based.There is a need to realize interfaces and integration betweenracetrack and CMOS and it requires aconverter.Generally, a racetrackconverter comprises offunctionalities of both nonvolatile memory and data converter.The importance of an interface circuit with CMOS mustrequire providing and sensing currents at input and output of converter respectively. Therefore, interface circuits primarily consists of sense amplifiers as well as voltage-current converter (*V–I)*for an ADC.

The speed of switching in the MJT is not really fast that meet the cache memory requirements of many hundreds of MHz frequencies. Because the switching in MTJ is associated with write operation and the speed of STT-MRAM's limited by write speed. In order to overcome this issue a new circuit technique and a background scheme in write operation has developed. Thistechnique attains very high-speed in write operation. And it is done by not showing switching time of MJT from STT-MRAM operation. The present proposed technique/concept is to realize background scheme of write operation the circuit of6 transistor and 2MTJ type using STT-MRAM cell.In proposed scheme, every STT-MRAM cell is being configured with MTJs and also with a commoncell in 6T SRAM. A write operation is carried out in High speed by CMOS latch using SRAM frequency of operation.To MTJs from CMOS latch (called as MTJ backup") is consequently performed apart SRAM frequency. MTJ and backup operation,STT-MRAM type 6T-2MTJ cells are suitable, since write operation of MTJ is done by making source line (SL) to float.

2T-2MTJ is the considered as smallest cell based on the combination of 1T-1MTJ in STT-MRAM differential type cell. Illustration on the 2T-2MTJ is: it is simple structured cell, that comprises of MTJs and selecting transistor.The results of removing CMOS latch and comparingit to primary differential STT-MRAM cell type is indicating the reduction in area of cell among differential type of memory.

Whenever this memory cell was given/connected to STT-MRAM, it is observed that operating speed degradation and it is concerned since removing latch that may provide equivalent high speed operability for SRAM.It was confirmed that prospect in attaining 500 ps read latency with the help of feedback sense amplifier and also optimizing array configuration of array cell based on circuit simulation analysis.

The voltage difference is present in the CMOS latches (SN, /SN) internal nodes. The performance of MTJs switching is automatically done by making current to flow in the pair of MTJ, and it is resulted if and only if the SL made to floating then SN and /SN makes voltage difference.As this operation is not a part in CMOS latch operations so it maintains speed and also attains the nonvolatile write operation in SRAM. One Mbit prototype of STT-MRAM is designed as well as fabricated using this scheme by CMOS 90nm standard and also extra MTJ process with 100nm technology.Finally it was summarizedas Write/read of 2.1ns/15ns was realized. It is sufficient enough to application of memory cache. Mark that MTJs write speed is relaxed to time sufficient will be switched.

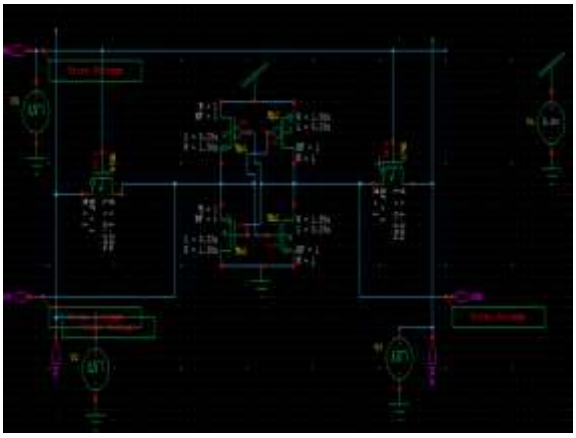

Fig.1: SCHEMATIC VIEW OF SPINTRONIC MEMORY

The nano wire of racetrack memory itself is a nonvolatiletype memory. Immediately just after data conversion the data is being stored in this nonvolatile racetrack without timing and area overhead. With the help of basic current sense amplifiers of CMOS,heolps out in accessing of stored data.Whenever the DWs midpoint is moved beneath read MTJ, it affects the difference in resistance in between the reference and read MTJs to very small.And this may results meta-stability effect in sense amplifier and errors are induced.Error becomes very significant as bits approach their flip point.In order to overcome multi-bit flipping, a gray code is used in the place of binary code in order to ensurechanges in one bit at a particular time.

IV. RESULTS

During conversion of data the proposed converter using racetrack works always in current mode.In Comparison other CMOS conventional voltage mode converter, a computational current mode suffersvery less noise.With the help of magnetic material, current-motion driven in DW is not really sensitive to temperature or magnetic fields and pinning. 10-year withholding at 150 °C hasendurances and achieved nearly 1010 cycles was reported a 109A/cm2 density of

write current in 90 nm technology, and that illustrates great reliability.

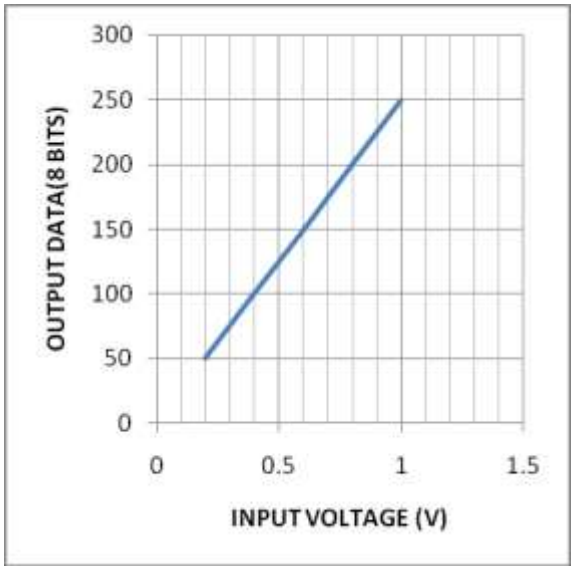

Fig.2: SIMULATED DATA CONVERSION IN ADC

This combination of excellent retention and higher endurance shows that this technology is very good match to nonvolatile conversion with higher sampling rates.

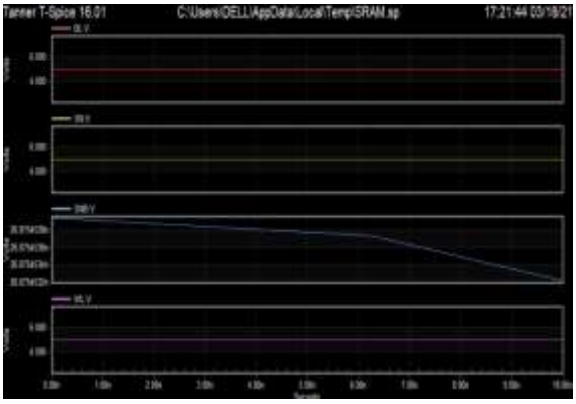

Fig.3:OUTPUT WAVEFORMS OF SPINTRONIC MEMORY

The above figure shows output waveforms of spintronic racetrack memory during read and write techniques. This improves the ADC to use low power as these techniques are quick operatives.

V. CONCLUSION

Low power ADC with transverse technique using spintronic racetrack memory device is proposed. This combination of excellent retention and higher endurance shows that this technology is very good match to nonvolatile conversion with higher sampling rates. The racetrack ADC converter which was proposed works only in current mode while data conversion. As compared with other voltage mode CMOS converter current conversional modes got less noise.Above outcomes points out those racetrack convertersare very useful in future small area low-power applications where multiple ADCs needed. Designing and executing Spintronic racetrack memory is done.

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