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Review Article

# REDUCED SWITCH TOPOLOGIES FOR MULTI LEVEL INVERTERS WITH M-CARRIER SPWM

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**Abstract**

This paper presents the transformer based multilevel inverter topologies with a m-carrier based level shift sinusoidal pulse width modulation method. Two topologies are presented in which the first topology has two bridges, one gives quasi square wave output and the other gives pulse width waveform. The outputs of two bridges are energized with the two different ratio transformers. The secondary terminals of two transformers are cascaded to attain 19 level output voltage wave form. The second topology has only one bridge and it contains 8 switches and two DC sources. The bridge output is given to the transformer and it acts as an isolation. The output of the topology gives the 7-level output. This topology has less number of components to reduce the cost and provides inbuilt isolation, to enhance the reliability of converter. The paper uses the common level shift SPWM method with modified carrier that is m-carrier to attain the maximum amplitude and the harmonics are shifted to very high level without change in the frequency. The paper topologies are validated with experimental results.

**Keywords:** Multi-level inverter, reduced switch, modified carrier.

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## INTRODUCTION

In recent past, multilevel Inverters are considered as the most important power converter for various applications, such as power-active filters, ac traction, direct grid integration systems, electric vehicles, etc. In reality, the quality of multilevel output voltage waveform is enriched as the number of levels moving high. Moreover, an appropriate switching strategy raises their potentiality in terms of good power factor, smaller filter size, improved efficiency, less voltage stress on power devices, and reduce energy waste. In current scenario, diode clamped MLI, flying capacitor MLI, and cascaded MLI are drawn more attention to accomplish the above-mentioned applications. However, to get the required number of output voltage levels by using less number of dc sources, power electronic switching components become a hectic job. In this view, many new inverter topologies with a claim of less device count are suggested in the literature. In the author suggested a cascaded transformer-based MLI with single dc supply. Herein, all H-bridges are connected to individual transformers to attain optimal output voltage levels. However, it has drawn a huge number of switches and heavy weight transformers. There are some problems with the conventional MLI's. Those are heavy size, when we are dealing with the more levels.

To overcome this problem, this paper presents a m-carrier based SPWM technique for a new reduced switching MLI.

The basic intention behind the implementation of a new control technique is to improve the magnitude and harmonic profile of load voltage. This paper topology uses the topology shown in [1].

The paper is organised as follows

Section II presents the topologies and working principle of 19 level inverter and 7 level inverter.

Section III represents the experimental results.

Section IV represents the conclusion

## 19-LEVEL INVERTER AND 7-LEVEL INVERTER

### 19-Level Inverter Operating Principle

The first topology single phase 19 level multilevel inverter topology is shown in Fig. 1. The converter model contains two bridges, Bridge A & Bridge B. Bridge A is a normal H-bridge and it generates 3 level output (quasi square wave). Where bridge B contains 4 extra switches with the normal H-bridge. The extra switches are used to attain different levels in the output. There are two supplies used in the topology are int he ratio of 2:1. The output of two bridges are connected to the primary side of the two different transformers, one is in the ratio of 1:2 and the other in the ratio of 1:1. The main intention of using the transformers is the get the maximum number of levels and the transformers provides the isolation from load to source. By use of transformers it helps reduce the number of switches, so that the size also be reduced. The secondary terminals of two transformers are cascaded to get the total output. The switching states of two bridge switches are tabulated in Table I.

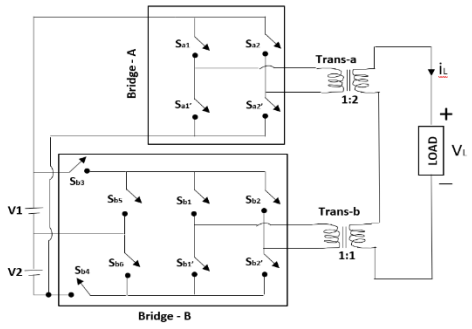


**Fig1: Schematic of the 19-level inverter**

1. First level (1L): Switches Sa1, Sa2 of Bridge A are ON so that it short the transformer terminals resulting in 0Vdc from Bridge A. Switches Sb1, Sb2', Sb4, Sb5 are ON, where sb4, sb5 switches connects the V2 suppy and resulting in Vdc from Bridge B. Total Voltage VA+VB=0+Vdc=Vdc.
2. Second level (2L): Switches Sa1, Sa2 of Bridge A are ON so that it short the transformer terminals resulting in 0Vdc from Bridge A. Switches Sb1, Sb2', Sb3, Sb6 are ON, where sb3, sb6 switches connects the V1 suppy and resulting in 2Vdc from Bridge B. Total Voltage VA+VB=0+2Vdc=2Vdc.

3. Third level (3L): Switches Sa1, Sa2 of Bridge A are ON so that it short the transformer terminals resulting in 0Vdc from Bridge A. Switches Sb1, Sb2', Sb3, Sb4 are ON, where sb3, sb4 switches connects across the V2 and V1 suppy and resulting in 3Vdc from Bridge B. Total Voltage VA+VB=0+3Vdc=3Vdc.
4. Fourth level (4L): Switches Sa1, Sa2' of Bridge A are ON so it gives 3Vdc and due to 1:2 ratio transformer, the output is 6Vdc. Switches Sb1', Sb2, Sb3, Sb6 of Bridge B are turned ON, where Sb3, Sb6 switches are leads to connect across V1 and due to Sb1', Sb2 are turned ON, the polarity is reversed and resulting in –2Vdc. Total Voltage VA+VB=6Vdc-2Vdc=4Vdc.
5. Fifth level (5L): Switches Sa1, Sa2' of Bridge A are ON so it gives 3Vdc and due to 1:2 ratio transformer, the output is 6Vdc. Switches Sb1', Sb2, Sb4, Sb5 of Bridge B are turned ON, where Sb4, Sb5 switches are leads to connect across V2 and due to Sb1', Sb2 are turned ON, the polarity is reversed and resulting in -Vdc. Total Voltage VA+VB=6Vdc-Vdc=5Vdc.
6. Sixth level (6L): Switches Sa1, Sa2' of Bridge A are ON so it gives 3Vdc and due to 1:2 ratio transformer, the output is 6Vdc. Switches Sb1, Sb2 of Bridge B are turned ON to short the 2nd transformer terminals and resulting in 0Vdc. Total Voltage VA+VB=6Vdc+0Vdc=6Vdc.
7. Seventh level (7L): Switches Sa1, Sa2' of Bridge A are ON so it gives 3Vdc and due to 1:2 ratio transformer, the output is 6Vdc. Switches Sb1, Sb2', Sb4, Sb5 are ON, where sb4, sb5 switches connects the V2 supply and resulting in Vdc from Bridge-B. Total Voltage VA+VB= 6Vdc+Vdc= 7Vdc.
8. Eighth level (8L): Switches Sa1, Sa2' of Bridge A are ON so it gives 3Vdc and due to 1:2 ratio transformer, the output is 6Vdc. Switches Sb1, Sb2', Sb3, Sb6 are ON, where sb3, sb6 switches connects the V1 supply and resulting in 2Vdc from Bridge B. Total Voltage VA+VB= 6Vdc+2Vdc= 8Vdc.
9. Ninth level (9L): Switches Sa1, Sa2' of Bridge A are ON so it gives 3Vdc and due to 1:2 ratio transformer, the output is 6Vdc. Switches Sb1, Sb2', Sb3, Sb4 are ON, where sb3, sb4 switches connects across the V2 and V1 supply and resulting in 3Vdc from Bridge B. Total Voltage VA+VB= 6Vdc+3Vdc= 9Vdc.
10. Zero level (0L): Switches Sa1, Sa2 of Bridge A are ON so that it short the transformer terminals resulting in 0Vdc from Bridge A. Switches Sb1, Sb2 of Bridge B are turned ON to short the 2nd transformer terminals and resulting in 0Vdc. Total Voltage VA+VB=0+0=0.

Similarly, the negative states also designed by changing the respective switching states of the Switches of two bridges. The main intension of using this type of is to reduce the number of switches and burden on the switches. The expected output of the inverter is shown in Fig 2.

**TABLE ITRIGGERING STATES OF 19 LEVEL TOPOLGY**

| Bridge A | Bridge B | Output |
|---|---|---|
| Sa1, Sa2(0Vdc) | Sb1, Sb2(0Vdc) | 0Vdc |
| Sa1, Sa2(0Vdc) | Sb1, Sb2', Sb4, Sb5(1Vdc) | 1Vdc |
| Sa1, Sa2(0Vdc) | Sb1, Sb2', Sb3, Sb6(2Vdc) | 2Vdc |
| Sa1, Sa2(0Vdc) | Sb1, Sb2', Sb3, Sb4(3Vdc) | 3Vdc |
| Sa1, Sa2'(6Vdc) | Sb1', Sb2, Sb3, Sb6(-2Vdc) | 4Vdc |
| Sa1, Sa2'(6Vdc) | Sb1', Sb2, Sb4, Sb5(-1Vdc) | 5Vdc |
| Sa1, Sa2'(6Vdc) | Sb1, Sb2'(0Vdc) | 6Vdc |
| Sa1, Sa2'(6Vdc) | Sb1, Sb2', Sb4, Sb5(1Vdc) | 7Vdc |
| Sa1, Sa2'(6Vdc) | Sb1, Sb2', Sb3, Sb6(3Vdc) | 8Vdc |
| Sa1, Sa2'(6Vdc) | Sb1, Sb2', Sb3, Sb4(3Vdc) | 9Vdc |

**M Carrier**

The carrier used in the first topology comes under the level shift carrier type for different levels. Again in level shift carrier type, it is categorised into three types. The topology uses the phase opposition disposition PWM technique. Where the carriers in positive and the negative are opposite in phase and every carrier is displaced by some DC offset according to the number of carriers. Normally the type of carrier which we used is either ramp or triangle signals. In the topology we used a different carrier. Generally when carrier frequency is increased, it shifts the lower order harmonics to higher order harmonics. As if it is still increasing the carrier frequency to very high, the switching states (dv/dt) is increases and EMI affects the operation. But if we reduce the frequency, the harmonics will be in lower order. In order to rectify that the topology represents a new m-carrier, so that without increase in frequency the comparisons of reference wave with the carrier wave is increases with the new carrier.

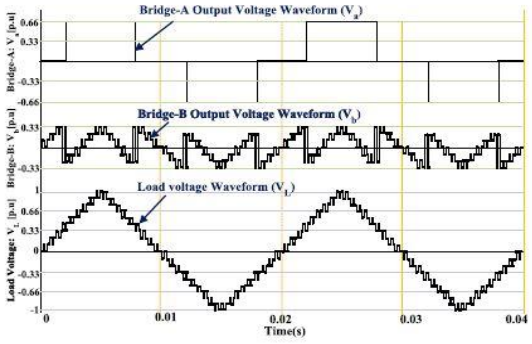


**Fig. 2: Output of the 19-level Inverter**

The modified carrier is discovered from the centre aligned carrier so called triangular waveform without changing the peak to peak magnitude and frequency of the carrier wave. Consider the triangle waveform with the frequency 1/Ts that splits equally into six parts by the time scale Ts/6 as like shown in fig. 3(b). If we compare the Fig. 3(b) and Fig. 3(e), where both the figures shows the comparison of reference wave and carrier waves having same peak to peak magnitude and same frequency. But when the comparison is done from Fig. 3(b) generates two pulses where in Fig. 3(e) generates four pulses without change in frequency. The difference between the values at the Ts/6 and at 2Ts/6 is considered as δ. For a normal triangle wave the δ value is negative, after checking the different values it is seen that δ at 0.45 gives the better output from different values. When δ is 1 the wave generates 4 pulses but resulting in triple frequency.

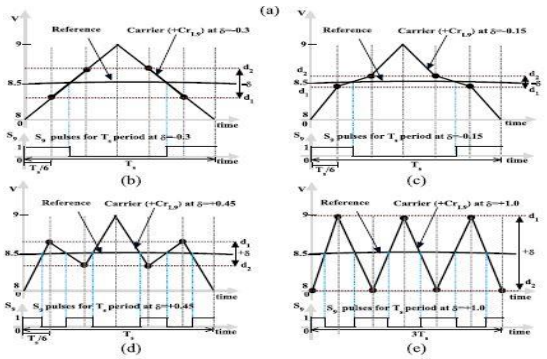


**Fig. 3. Generating the modified carrier**

The same carrier waves are generated with some DC offsets according to the 19 level inverter. In 19 level inverter it needs 9 carriers in positive side and another 9 carriers in negative side with phase opposition. The comparison block for a single wave is shown in Fig. 4(a). Where 1 is the carrier frequency and 2 is the reference frequency. The system is designed as the pulse is generated only when the comparison of two waves are in the limits of the specific carrier wave peak to peak and lower limit.

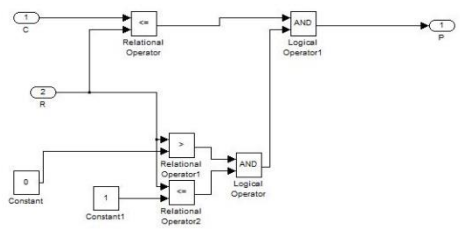


**Fig. 4(a). Generation of PWM for a single block in MATLAB Simulink model**

As we can observe form the Table II, that the switching states of all switches are not in sequence. For that, it needs extra circuitry to generate the PWM pulses. The extra circuit is shown in Fig. 4(a). The extra logic block used to generate the PWM pulse in the range of that comparison level only. Using the DC offset values, remaining carriers are generated and the Fig. 4(a) model is converted into subsystem and given to every carrier wave. The total carrier wave generation and comparison are shown in Fig. 4(b). The generated waveforms are shown in Fig. 4(c).

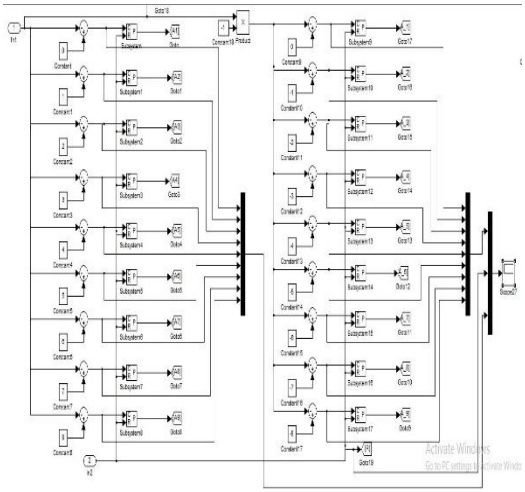

**Fig. 4(b). MATLAB Simulink model of generation of carrier waves and PWM**

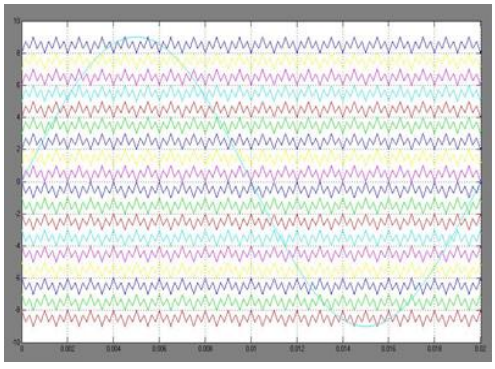

**Fig. 4(c). 18 Carrier waveforms for 19 level inverter**

From Table. I it is observed that the switching period of the switches are not in sequential order. The ON time states of the Switches are listed in Table. II. The numbers in the table shows the different levels. In order to get the specific switching pulse. The combination of respective level pulses are given to the OR gate. So that the respective switching logic is attained. The MATLAB model is shown in the fig.5.

**TABLE II ON STATE LEVELS OF SWITCHES IN 19 LEVEL TOPOLOGY**

| Switches | Positive Half Cycle | Negative half Cycle |
|---|---|---|
| Sa1 | 1,2,3,4,5,6,7,8,9 | -1,-2,-3 |
| Sa2 | 1,2,3 | -1,-2,-3,-4,-5,-6,-7,-8,-9 |
| Sb1 | 1,2,3,6,7,8,9 | -4,-5 |
| Sb2 | 4,5,6 | -1,-2,-3,-7,-8,-9 |
| Sb3 | 2,3,4,8,9 | -2,-3,-4,-8,-9 |
| Sb4 | 1,3,5,7,9 | -1,-3,-5,-7,-9 |
| Sb5 | 1,5,7 | -1,-5,-7 |
| Sb6 | 2,4,8 | -2,-4,-8 |

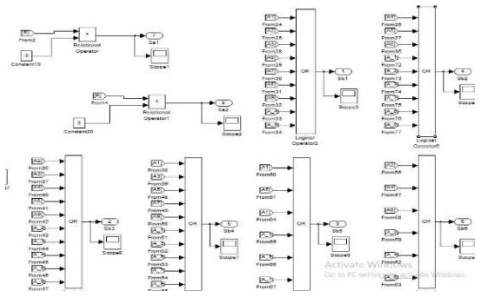

**Fig. 5. Combining level pulses to get Switch Pulse**

Now the pulses are ready to give the switches. These blocks are modelled into subsystem and the inputs of the subsystem are reference wave and the carrier wave. The output of the block are pulses of the 8 switches. The remaining switches Sa1', Sa2', Sb1', Sb2' are the compliment of the switches Sa1, Sa2, Sb1, Sb2 respectively and they can be generated simply by adding a logical NOT gate to the switch pulses. When these pulses are given to their respective switches according to the modulation index (ma) it generates the multilevel inverter output, where bridge A generates quasi square wave and bridge B generates different level outputs. When ma=1 the inverter generates 19 level output voltage and that is shown in fig. 6. In that model carrier frequency is taken as 1.5KHz. Single level voltage is taken as 15 volts, so, for 19 level positive side peak voltage is 135 volts and negative side is -135 volts. The type of level shift carrier used in the model is Phase Opposition Disposition (DOP) type, where the positive side and negative side carriers are opposite in phase that means both are mirror image to each other. This type of carrier is used because to get more symmetricity in the output waveform.

To validate the topology the MATLAB Simulink model is done, where carrier frequency fc is taken as 1.5KHz, single level voltage Vdc is taken as 15 volts. The output is shown in fig. 6. From the output voltage wave form and from the Table V maximum burden is on bridge A comparative to bridge B. The transformers are not only meant for to attain different levels it also provides the isolation from load to source and itself acts as the protective circuit.

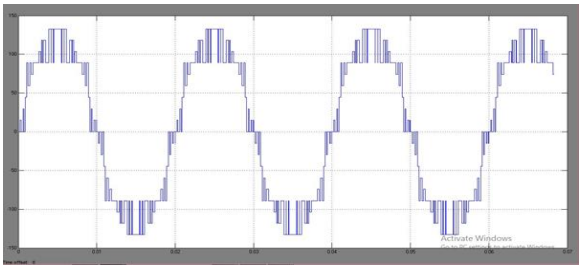

**Fig. 6 Output Voltage of the Inverter (19 level)**

### 7-Level Inverter Operating Principle

The second topology is 7-level Inverter. In this topology it contains only single bridge with extra four switches and two DC sources and one Isolation transformer. The extra four switches help to attain more levels. If we use normal cascaded MLI for 7-level inverter, it requires 12 switches in the circuit. Here with the use of 8 switches we can get 7 levels. The circuit is shown in Fig. 7 contains two DC sources V1 & V2 are in the ratio of 2:1. The transformer is used as a isolation purpose from load side to source side. To attain 7-levels, the switching states of all switches in the circuit are tabulated in table III.

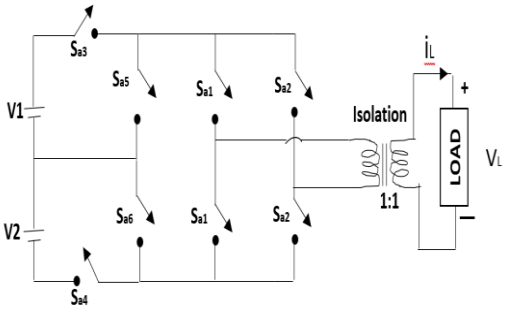


**Fig. 7. Schematic of 7-Level Inverter**

1. First Level(1L): Switches Sa1, Sa2 are ON so that the transformer terminals are shorted or we can open the Sa3 and Sa4 switches so that the supply is blocked resulting in 0Vdc.
2. Second Level(2L): Switches Sa4, Sa5, Sa1, Sa2' are ON so that the transformer is connected to V2 source that is 1Vdc resulting in output voltage of 1Vdc.
3. Third Level(3L): Switches Sa3, Sa6, Sa1, Sa2' are ON, so that the transformer is connected to V1 source that is 2Vdc and resulting in the output voltage of 2Vdc.
4. Fourth Level(4L): Switches Sa3, Sa4, Sa1, Sa2' are ON, so that the transformer is connected across the V1 and V2 sources that is 3Vdc and resulting in the output voltage of 3Vdc.
5. Fifth Level(-1L): Switches Sa4, Sa5, Sa1', Sa2 are ON, so that the transformer is connected across the V1 source with reverse polarity that is -Vdc and resulting in the output voltage of -Vdc.
6. Sixth Level(-2L): Switches Sa3, Sa6, Sa1', Sa2 are ON, so that the transformer is connected across the V1 source in reverse order that is -2Vdc and resulting in the output voltage of -2Vdc.
7. Fourth Level(-3L): Switches Sa3, Sa4, Sa1', Sa2 are ON, so that the transformer is connected across the V1 and V2 sources in reverse polarity that is -3Vdc and resulting in the output voltage of -3Vdc.

**TABLE IIITRIGGERING STATES OF 7 LEVEL INVERTER TOPOLGY**

| Levels | ON Switches | Output |
|---|---|---|
| 1 | Sa4, Sa5, Sa1, Sa2'(1Vdc) | 1Vdc |
| 2 | Sa3, Sa6, Sa1, Sa2'(2Vdc) | 2Vdc |
| 3 | Sa3, Sa4, Sa1, Sa2'(3Vdc) | 3Vdc |
| 4 | Sa1, Sa2(0Vdc) | 0Vdc |
| 5 | Sa4, Sa5, Sa1', Sa2(1Vdc) | -1Vdc |
| 6 | Sa3, Sa6, Sa1', Sa2(2Vdc) | -2Vdc |
| 7 | Sa3, Sa4, Sa1', Sa2(3Vdc) | -3Vdc |

There are total eight switches in the circuit. The switches Sa3, Sa4, Sa5, Sa6 are used to trigger the different levels. The switches and the complement switches of Sa1, Sa2 are acts like a normal H-bridge inverter. As like in 19-level inverter model, 7-level inverter model also has no sequence of Switching. The Switching states of all the switches are tabulated in Table IV.

**TABLE IV ON STATE LEVELS OF SWITCHES IN 7 LEVEL TOPOLOGY**

| Switches | Positive Half Cycle | Negative half Cycle |
|---|---|---|
| Sa1 | 0,1,2,3 | |
| Sa2 | 0 | -1,-2,-3 |
| Sa3 | 2,3 | -2,-3 |
| Sa4 | 1,3 | -1,-3 |
| Sa5 | 1 | -1 |
| Sa6 | 2 | -2 |

As like in the 19-level inverter topology, 7-level inverter also uses the m-carrier SPWM technique to shift the harmonics to very higher order. The pulses are generated just like in the 19-level topology but with reduced carriers. The logic of developing the 7-Level inverter topology is same as 19-level inverter topology. The use of 7-level inverter topology is to reduce the number of switches and only one transformer is used. It can be used when we use the switches having more peak inverse voltage and when the loads are more inductive in nature.

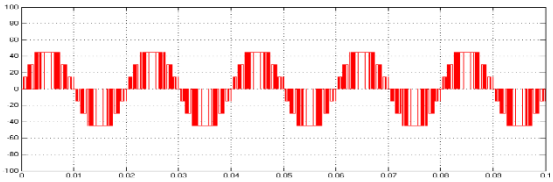

**Fig. 6 Output Voltage of the Inverter (7 level)**

The above fig. 6 shows the output of matlab model of 7 level-inverter with carrier frequency of 1.5KHz and level voltage of 15V. As there are two sources in the circuit, one is 15V and the other source is 30V.

### Comparison with Other topologies

The comparison of this topology with the other recent hybrid MLI based on the number of switches, transformers, PIV, number of DC sources and number of levels achieved are tabulated in Table IV. By seeing the table one can say that this topology is the best because the PIV (peak inverse voltage) of the switch is 3Vdc where as in other inverters it is 9Vdc and 7Vdc. We are going for multilevel inverter to reduce the PIV because when we go for high PIV switches the dv/dt is very high. According to the number of the transformers used, we used only two transformers where as in other topologies there 9 transformers and it leads to the heavy size of the inverter and more packing size. The number of switches are very less compared to other topologies to attain maximum number of levels. As the number of switches are reduced, the number of gate drivers are also reduced automatically so that the inverter size is also reduced.

**TABLE VCOMPARISON WITH OTHER TOPOLOGIES**

| Factors | [2] | [3] | [4] | [5] | [6] | 19-level |
|---|---|---|---|---|---|---|
| Levels | 11 | 19 | 19 | 19 | 15 | 19 |
| Sources | 1 | 1 | 1 | 5 | 3 | 2 |
| Switches | 12 | 20 | 20 | 14 | 12 | 12 |
| Transformers | 3 | 9 | 9 | 0 | 0 | 2 |
| PIV | 1Vdc | 9Vdc | 1Vdc | 9Vdc | 7Vdc | 3Vdc |

## EXPERIMENTAL RESULTS

To validate the results, a hardware setup was built with the inverter modules. IGBTs are selected for power switches, gate driver circuits, protection circuits are also shown for Bridge A of the considered topology in the fig. 7. Similar structure is employed for Bridge B. DC source of 20V considered for Bridge A and 40V for Bridge B. Carrier frequency is considered as a 1500Hz, reference is taken as grid frequency(50Hz). Control logic is implemented using Artix 7 FPGA based digital controller.

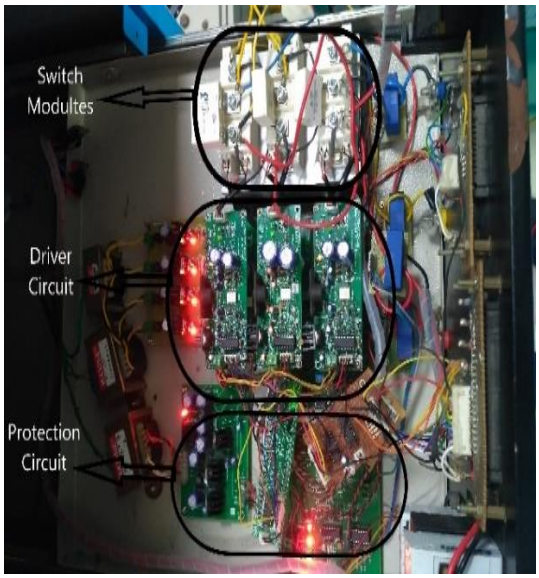


**Fig. 7 Experimental setup**

**DESIGN SPECIFICATIONS**

| Parameter | Value |
|---|---|
| IGBT | 1200V |
| Switching frequency | 1500Hz |
| Driver circuit | 316J |
| Transformer 1 | 1:1, 2KVA |
| Transformer 2 | 1:2, 2KVA |

The Fig. 8,9,10 shows the output voltage waveforms of Bridge A, Bridge B and the inverter output respectively. Fig. 8 shows the output voltage waveform of Bridge A, which is in the form of quasi square wave and helps to give the dc offset of the Bridge B. Fig. 9 shows the Bridge B output voltage waveform symmetrical different levels to get maximum number of inverter levels. Fig. 10 shows the output waveform of the inverter which is the cascaded output of Bridge A and Bridge B and gives the 19-level output for ma=1.

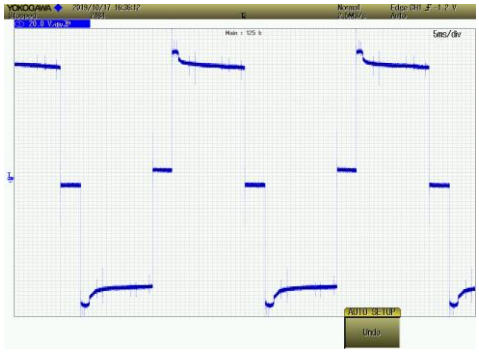

**Fig. 8 Output voltage waveform of Bridge A**

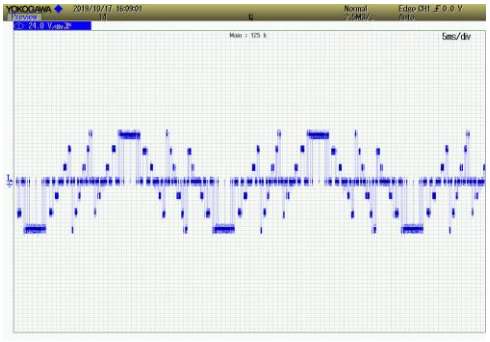

**Fig. 9 Output voltage waveform of Bridge B**

**Fig. 10 Output voltage waveform of Inverter**

## CONCLUSIONS

Flexibility of the topology to achieve many discrete levels with a maximum of 19 levels with minimum number of switches is highlighted in the paper. Modification of carrier is proposed which apparently increases switching frequency by twice or thrice. As the number of levels increases the output voltage nearer to the reference wave (sinusoidal wave) so that the THD will move to very higher order harmonics and that leads to the low size of the filter. If the load itself is the inductive in nature, then there is no need of the filter. It is used for the speed control of Megawatt drives, grid integration, ac traction, electric vehicles.

## ACKNOWLEDGEMENT

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