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A Novel Design of Ultra-Low Power 32/33 Prescaler based on modified 2/3 TSPC Prescaler for PLL Applications

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Abstract:

In this paper the power consumption and speed of Razavi and TSPC DFF based Frequency divider are investigated. Based on this investigation to develop proposed TSPC based 2/3 prescaler with low power consumption with the help of eliminating in-between AND, OR logic is replaced by only 3 transistors. A divide-32/33 dual modulus Prescaler is implemented with this proposed 2/3 prescaler using GPDK 180nm CMOS process technology. The results re compared with previous work and is capable of operating 4.1 GHz with 1.49mW power consumption.

Keywords: Prescaler, High Speed, Low Power, TSPC, Frequency Divider

1. Introduction:

The dual modulus is very important and critical block in frequency synthesizer, which operates at highest frequencies and consumes more power than other blocks. The Prescaler are formed by DFF and additional logic. The CML [1] based Prescaler is working at 13 GHz but consume more power. The extended TSPC (E-TSPC) is faster than TSPC but power consumption is more [2]. The proposed Prescaler are suitable for pulse swallow topology and modular topology [3] [4]. In the pulse swallow topology required two more counters namely p-counter and s-counter. In the modular divider topology requires some control signals such as mod and p [4] these are made small modification in 2/3 prescaler design. Without static power dissipation TSPC Prescaler consume low power among the different topologies so different kind of TSPC Prescaler are proposed for reduce critical path delay [6] for reduce logic gates and for reduce stacking stages but there is trade of between speed and power consumption. While maintain the this trade off we present new 2/3 prescaler that improves power consumption.

2. Traditional Divider Architecture:

This paper utilizes the flip-flop-based circuit to understand the frequency divider. The main topology is Behzad Razavi, topology [1] , it comprises of two latches associated in master and slave setup. Every Flip-Flop is activated by two correlative clock signals Clock and Clock bar.The another topology is TSPC divider topology [2] which is shown Fig. 1.This topology is based on D Flip Flop, it required only single phase clock either ClK or ClKB and only 9 transistor are used.Fig. 4b shows three stage of nine transistor provide high speed and the operating frequency range also high so TSPC is more appropriate architecture for frequency divider operation. However TSPC is require full voltage swing contrast to Razavi to achieve high frequency.

3. Design of proposed 2/3 Prescaler:

The problem of traditional 2/3 Prescaler is both DFF is activate at half of the clock even if one of the DFF not involve divide by 2 mode so the shortcircuit power and switching power occur unnecessarily. So the proposed design eradicates this problem mainly. The proposed design consists of two DFF (TSPC), 2 PMOS and 1 NMOS transistor. In this method main modification was instead of using AND gate, use pass transistor logic. The division control MC is implemented using PMOS and AND gate functional is made by two transistors as shown in Fig.2

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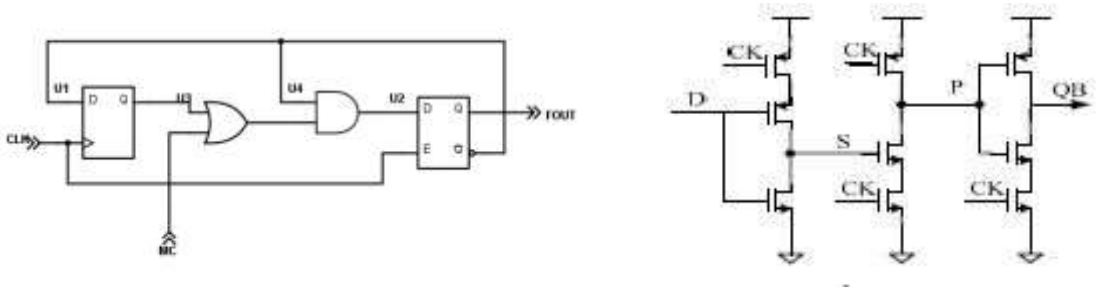

(a) **Conventional 2/3 Prescaler** **b)Schematic of the TSPC DFF**

Fig. 1: Conventional 2/3 Prescaler

$$Fout = MC \times \frac{Fin}{3} + MC \times \frac{Fin}{2} \quad (1)$$

when MC=0 PMOS is always on , equal to logic Q and Q is the input of NMOS and gate control is Qb , drain is connected to DFF2(U16) .PMOS input is always gnd , a control signal is same as Qb and drain are connected to DFF2(U16) so strong signal is drive the DFF2(U16). Such that Prescaler in the divide-by-3 mode. When MC=1 PMOS is always off so the input of NMOS and PMOS is depended on DFF2(U16) inverted output Qb so DFF2(U16) alone perform divide-by-2 mode**.**

4. Design of high speed dual modulus Prescaler:

To assist confirm the upsides of the proposed ultra-low power prescaler [5], a division 32/33 dual modulus unit is executed with the usage of 2/3 prescaler as appeared in Fig. 2. The low power based 32/33 prescaler as shown Fig. 3, consist of one proposed 2/3 prescaler unit and it is trailed by four phases of the TSPC based divide by-2 modules.At the point when the control signal MC is consistently high, the 32/33 prescaler capacity as division by-32 unit and the control signal MC to the 2/3 prescaler goes legitimately high permitting it to work in divide by-2 mode for the entire 32 clock cycles.Since control signal MC is legitimately high, DFF1 in the proposed 2/3 prescaler is totally worked for the whole 32 duty clock cycles. At the point when control signal MC is legitimately low, the 32/33 prescaler unit capacity as divide by-33 unit which 2/3 prescaler works in divide by-3 mode for 3 duty cycles and in division by-3 mode for 30 duty clock cycles which DFF1 in the proposed 2/3 prescaler turns off totally consequently decreasing the power utilization of 32/33 prescaler utilizing proposed 2/3 prescaler.

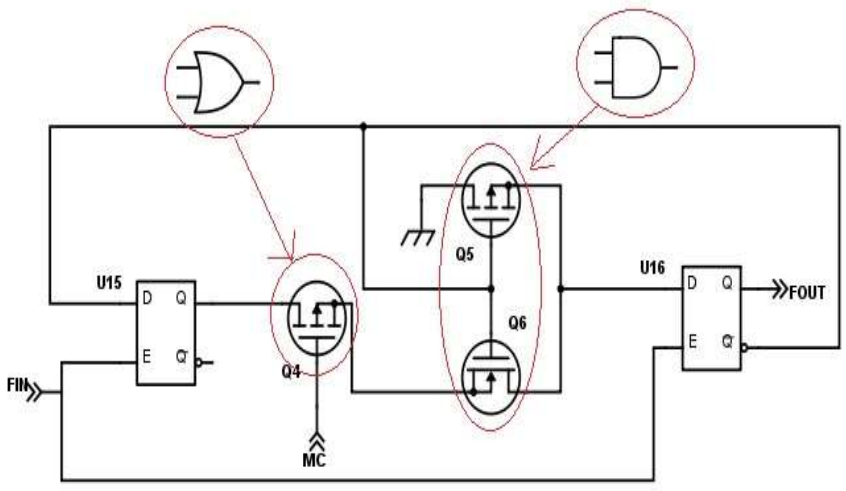

Fig. 2: Proposed 2/3 Prescaler Using TSPC DFF

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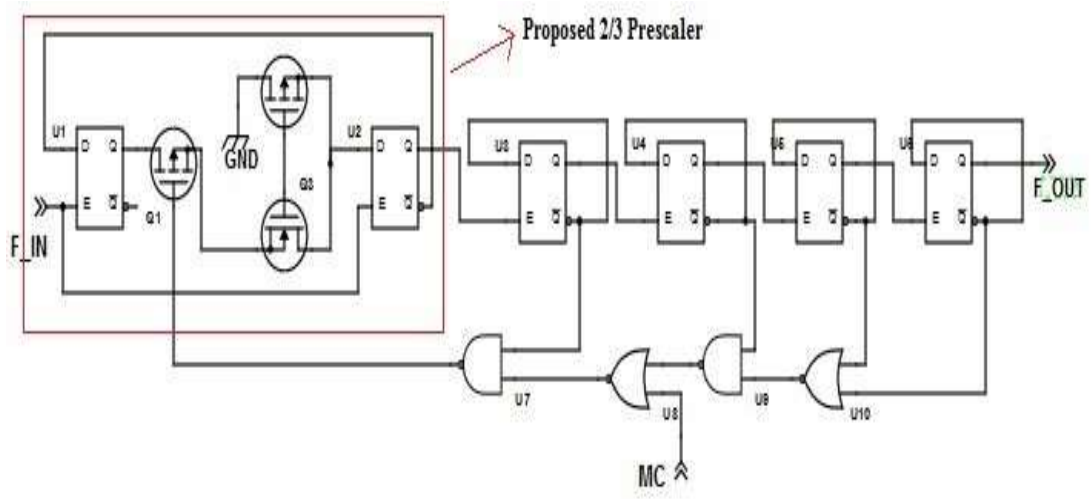

Fig. 3: Design of 32/33 Prescaler Using proposed 2/3 Prescaler

5. Simulation results:

A complete design and simulation of the proposed 32/33 prescalers are performed utilizing Cadence virtuoso for 0.18um CMOS process technology Fig 4a and 4b demonstrates the deliberate yield waveform of the 32/33 prescaler at 4 GHz frequency in divide by-32 and divide by-33 mode respectively. Fig. 4c demonstrates the deliberate power utilization against frequency of operation of the 32/33 prescaler. The measured most extreme working frequency of proposed prescalers is 4.1667 GHz.

a)Divide-32 b)Divide -33

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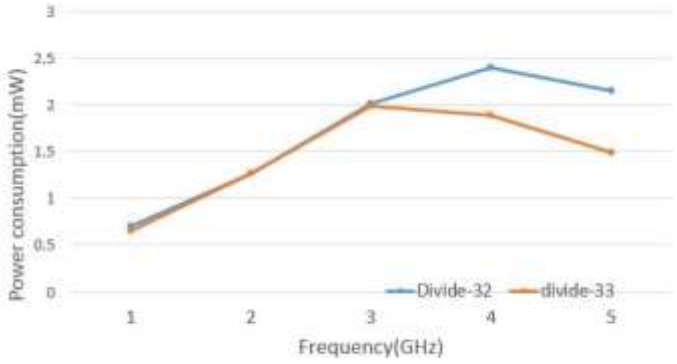

c) Frequency Vs Power consumption

Fig. 4: Output waveform for 32/33 Prescaler

6. Conclusion:

In this paper, a new high speed and low power based 2/3 prescaler is presented. The transistor logic is used instead of gate based to achieve. So the stacked delay and switching nodes are reduces and with 1 MHz resolution of 32/33 prescaler. It operates at 4.1 GHz maximum with consume 1.49mW power. The functionality and performance were verified using cadence virtuoso 0.18um CMOS process technology.

7. References

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