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DESIGN OF HIGH PERFORMANCE AND FUNCTIONAL VERIFICATION OF DSP BOARD USING VLSI ARCHITECTURE

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ABSTRACT: The Field programmable gate arrays is used for many applications such as designing of Digital signal processing boards (DSP) and Application Specific integrated circuits (ASICs). Design of high performance and complex functionalities of boards are increasing computation cost and time consuming. In this paper, we provide functional verification of DSP board with high performance using Verilog Hardware description language architecture model. This is an automated and self functioning mode with complex functionalities. This work discuss about functional verification of DSP board using VLSI and Matlab. We can reduce and change number register and critical parallel input/output operations. This is pipeline based model so easily change the stage and adopt for any mathematical operations. The architecture is verified by existing functionalities and working environment.

KEY WORDS: Digital signal processing boards, VLSI Architecture, Matlab simulations, Functional verification, Performance

I. INTRODUCTION

To meet consistently expanding utilitarian necessities, advanced VLSI plans are getting mind boggling. Configuration groups are pressing more and more rationale doors onto a solitary chip to accomplish wanted usefulness and execution inside the predetermined impression [1]. Useful check of such plans with convention approach of utilizing coordinated test seats doesn't give adequate certainty inside given time plan. Test seats composed in VLSI gives focal points in wording empowering compelled irregular upgrade age, self-checking and declaration based check alongside characterizing useful inclusion grid [2].

Irregular computing methods are improves efficiency compare with manual testing based on number of vectors delivered and creates test results not unequivocally given by use case designers. An official attestation to a structure during recreation stage recognizes configuration blemishes progressively and decreases troubleshooting time essentially over non-attestation based plan. The DSP board are verified and improvements are verified by using complex functionalities. [3].

This method out to be significantly all the more trying for a locally available plan executing different DSP boards having functionalities, for example, sine/cosine method, input query table, drifting point transformation and the other way around, FFT, FIR channel, and so on. DSP calculations are accessible as standard capacities in MATLAB. In the event that these capacities can be utilized in the test bed as given as good checking results, the test seat can be rearranged and by and large proficiency of the check can be essentially improved [4].

This paper examines the check condition advancement utilizing DSP function and procedure to couple MATLAB with VLSI. This paper organizes as follows, section 2 discusses about various studies and literature about VLSI architecture, section 3 describes our proposed model, section 4 explains implementation and simulations and section 5 discuss about conclusion.

II. RELATED WORKS

Huang et al, flipping Discrete wavelet transform is applied for verifying multiple delays in networks. The pipeline model is suggested for stage by stage processing. The number of stages and registers are used to compute the performance. The estimation of all the computing boards is tested by using complex functions and outcome rate is also monitored. In this

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case the major problem is memory size and hardware computation time [5]. So this model we could not change the model while updation and reconfiguration.

The utilization and performance are two factors for any computer architecture models. The size of the board and components are important role players. Wong et al, the filtering and higher adequacy are to be changed and apply wavelet transform to performing multiplication operations. The problem is memory optimization and relocation. In case any new request or process in execution stage means need to test the computation overhead time [6].

The boards are implemented by using on-chip memory model and utilization is measured by using simulators. The structure and design of the board has low multifunction factor and components. The multiplier delay and long computation process is major problem in combinational circuit design. The pipeline structure may be reduce this issue but problem is verifying next hop values or computational cost of each pipeline stages [7] [8].

III. PROPOSED MODEL

Confirmation of a VLSI configuration comprises of two significant advances. i). improvement of architectural design, ii). Examination of the structure reaction. In improvement stage, the pipelines is arranged by specific modes and upgrade it. In investigation part, the genuine check is performed. An example, testing of DSP boards are performing both these activities consequently is represented in Figure 1.

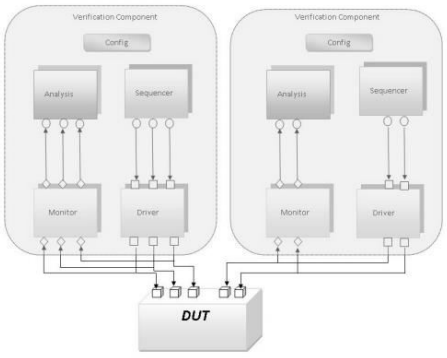

Figure 1 Functional Verification of VLSI Model

The test seat (check condition) created in VLSI utilizing UVM is made out of reusable check condition called check parts. Every segment is epitomized, prepared to-utilize, and configurable which can be utilized for check of any interface convention, plan sub module framework. The confirmation of each parts can be tested by using MATLAB simulator and conversion plan is designed.

The examination segment appeared in below figure 2, comprises of parts that watch conduct of the functional verification of our proposed model. The major parts for examination segment are inclusion assortment and DSP board scorecards. A scorecard decides if the plan is working appropriately or not. The scoreboard design isolates its assignments into two sub modules of concern viz. forecast prediction and assessment.

Figure 3: Analysis component and Matlab predictor value

An indicator model, in some cases alluded to as a 'Brilliant Reference Model', gets a similar improvement of functional verification boards and produces known reaction exchange functions. The indicator executes the functional codes

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usefulness at a higher level of reflection written in C, Python, C++ or Assembly codes. After the right usefulness is anticipated, the scoreboard can assess the real outcomes saw on the functional verification with the anticipated outcomes

The following methods are taken into account for MATLAB functions,

a. Direct interface: This is MATLAB engine which has programming interface and coding models, Linear equation mention below x and y are input functions and a,b are test bed, H and L factor for HDL verifiers,

$$y^{(2n+1)} = x^{(2n+1)} + a\,[\,x^{(2n)} + x^{(2n+2)}]$$

$$y^{(2n)} = x^{(2n)} + b\,[\,x^{(2n-1)} + y^{(2n+1)}]$$

$$H^{(2n+1)} = y^{(2n+1)} + c[y^{(2n)} + y^{(2n+2)}] \;\&\; L^{(2n)} = y^{(2n)} + d[H^{(2n-1)} + H^{(2n+1)}]$$

b. HDL Verifier: The Matlab tool box provides digital logic and programmable module. The verilog code is shown in below

```
a= [0:0.5:5]; b = 2*a.^2 + 3*a -5; c = 1.2*a.^2+4*a-3;
hold on p
lot(a,b,'-or',x,'g','y',2)
 plot(a,c,'--ok','g','c','I',2) xlabel('X'); ylabel('Y');
 legend('c1','c 2',1,'NW')
plot(a,b,'or','x','g',y,2)
plot(a,c,'ok','y','c','x',2)
xlabel('X'); ylabel('Y');
 legend('c1','c2',I','NW')
function outcome = myfunc1(x),y
outcome = 2*x^2 + 3*y + 7;
subplot(1,2,1)
plot(a,b,'-or','x','g','x',2) xlabel('X'); ylabel('Y');
legend('c ',I','Nw)
subplot(1,2,2)
plot(a,c,'--ok','x','c','I',2)
xlabel('X'); ylabel('Y');
 legend('c2',I','NWt')
for n = 1:5 x = n*0.1; z = myfunc1(x);
fprintf('x = %4.2f f(x) = %8.4f \t',x,z)
end
fID1 = fopen(output.txt','w'); for n = 1:4 b1 = n ; b2 = n^2 ; b3 = n^3;
fprintf(fID1,'%7u %7u %7u \r', b1,b2); end
```

Table 1: Functional Verification code block

The proposed function verificaiton handling component design is appeared in Figure 4. It is conceivable to apply this design in the line and section channel by the correct choice of RAM or on the other hand cushion appropriately. By embracing the two information/two yield basic plan, it is conceivable to diminish the design cradle size of each segment processor and column values of each processor and additionally improvement in speed of activity. At the point when segment channel begins its obligation, the info test getting from preprocessing module, the odd example xi (2n + 1) and the even example Xi (2n) are sending to section channel simultaneously in each cycle. Here I is the record input, n is output quantity with k.

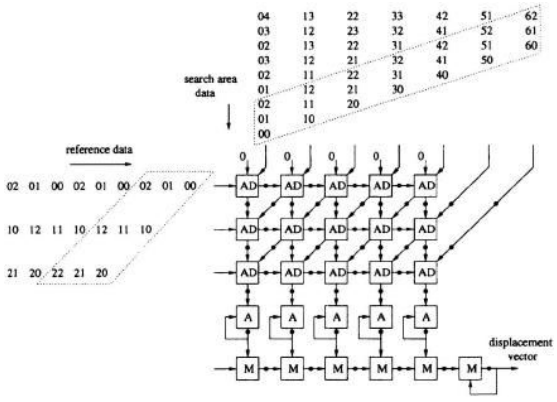

Figure 4: Proposed architecture with Functional verification and Matlab code

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IV. IMPLEMENTATION

The main structure is a DSP board of complex Fast Fourier transform model and length is 10452. The MATLAB computation is applied for FFT calculation and functional verification. The computational cost is calculated and tests the results. The verification of each functions using calmor model and analyze the performance. The plot of components and each function are two different testing elements. The design pattern and computation of each recurrence relations are shown in figure 6.

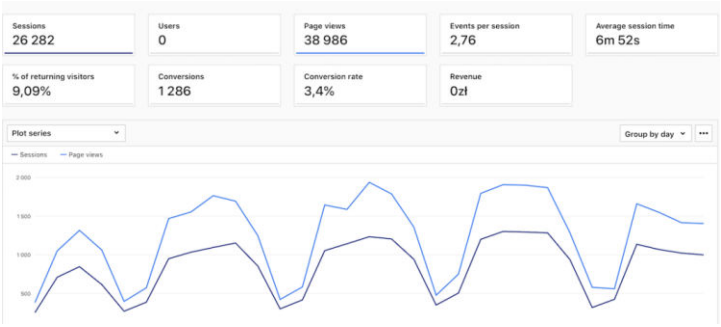

Figure 6: Recurrence relation of each iterated values.

The configuration is done by using sine and cosine model. MATLAB simulation produced 8 bit test bed and address the our proposed plans. The each functional representation and flip flop are used and available are noticed. C programming is used for functional verification process. Here, the 32-bit length boards are placed and 8-bit assigned for each functional operations. The below table 2 shows that device utilization of our model.

Logic Utilization	Used	Available
Representation of each chips	1568	5405
Flip Flop slices	128	512
Functional verification code blocks	387	1024
Bounded I/O operations	646	2048
RAM utilization	15	85
Clock size for computation	27	145

Table 2 Device utilization of proposed model

V. CONCLUSION

The high performance and functional verification board is designed using VLSI. It is self-checking useful check technique has been utilized to guarantee the utilitarian accuracy of DSP boards with complex functions. Utilization of this methodology empowers confirmation of each complex function of DSP board with lesser time computations. The MATLAB is utilized to create some particular information improvement each functional signals, which are hard to create in verilog. It is additionally plausible to complete expanded examination of the MATLAB utilizing range examination, separating at various levels.

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