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UPQC BASED SFCL FOR POWER QUALITY IN A DISTRIBUTION POWER SYSTEM

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Abstract:
The present power sector faces problems of low energy quality and the reason behind this low power quality is variations in voltage, harmonics, transients and demand for reactive electricity. The requirements today have increased a large share of power from power electronics and have raised the question of low power quality by connecting grids with wind farms and solar farms. Development and output evaluation on the basis of a superconductive fault current limit (SFCL) voltage sag compensation scheme. To order for incorrect voltage components to be completely paid, a prepayment technique is implement to lock the instantaneous sizes and phase angles of real-time line voltages. Thus UPQC is largely responsible for improving power quality and it demonstrates that the above listed problems are compensated for quite well. UPQC is therefore known as an effective solution to the problems of power efficiency. The simulations showed that the compensation voltage drop is in a position to preserve the root-middle-square voltages stabilizations and to minimize the adverse effects on sensitive load from the voltage drop. In addition, the compensated power induced responsive loads is decreased byUPQC, which reduces the cost of the capital in UPQC, due to the further voltage improvement generated by SFCL.
Key words: UPQC, standard of power, SFCL and voltage-sag compensation.

I.INTRODUCTION

The last few years have a highly Promising tension reduction compensation system was investigated and technologically demonstrated in [1] – [6] based in DVR (Dynamic Voltage Recovery) fitted with superconducting magnet storage (SMES). For instance the Nott magnet and its matching 150 kava power source (CSC) converter have been developed for protecting critical voltage loads of 110 kVA against slits in[2]. Two common magnets with HTS SMES are the Japanese 7.87-H/1-MJ/0.5-MVA magnet[5] and BSCCO 6.28-H/1-MJ/0.5-MVE[7] magnets with Chinese magnet magnets[1]. The cost of SMES coils' capital expenses[7] indicates that in reality an excellent idea of HES may also be more effective,[7][10] but SMES-based DVR systems are inefficient compared to conventional Battery Energy Storage (BES) equipment. The SMES systems have been designed in the future for the first time. The kW class of HES-based DVRs was shown during our previous works in [11]-[13] and integrated with the rapid reaction function of the SMES and with a BES-high power feature. A SMES-based DVR in MW-class will also be proposed and evaluated thereafter. In all threesome DVR systems, however, SMES needs high power or energy storage, particularly to offset strict voltage drop.

Nonetheless, the Superconducting failure current limit (SFCL) in the [14]–[18] distribution power system is validated to help balance the decrease in voltage. In our past research[20], we proposed and examined a resistive form of SFCL, which automatically starts and auto-applies the Double Fed Induction Generator(DFIG) to enhance failure driving.

A SMES-based, SFCL-resistive DVR system of the MW class would therefore be added to minimize the negative effects of voltage saving on sensitive loads. This system is described as its fundamental topology and technical theory, the parameter SMES and SFCL, DVR control strategy and simulation tests. This system is specified in detail. Furthermore, the optimum efficiency value is seen as minimizing the voltage sag device with respect to the DVR output power in the case of distribution line failure.

ISSN- 2394-5125 VOL 7, ISSUE 04, 2020

II. EXISITNG SYSTEM

Fig. 1(a) Shows the overall circuit topology for SMES-based DVR and SFCL. The DVR on the sensitive load side consist mainly of one SMES magnet with chopper, VSC, LC filters, in- grid transformers, a DC link condenser and a SMES unit. The DVR is composed of a SMES-based DVR is shown in fig.1(b). SFCL is thus correlated with other series feeders. The deletion of voltage for sensitive loads mainly results from the SFCL cooperation with SMES. In case of a three phase failure in a feeder that doesn't supply the sensitive load, the SFCL reduces the defect current and raises the typical bus voltage slightly. After the voltage is detected, the SMES-based DVR has been triggered, thus preserving the constant terminal voltage of the responsive charge.

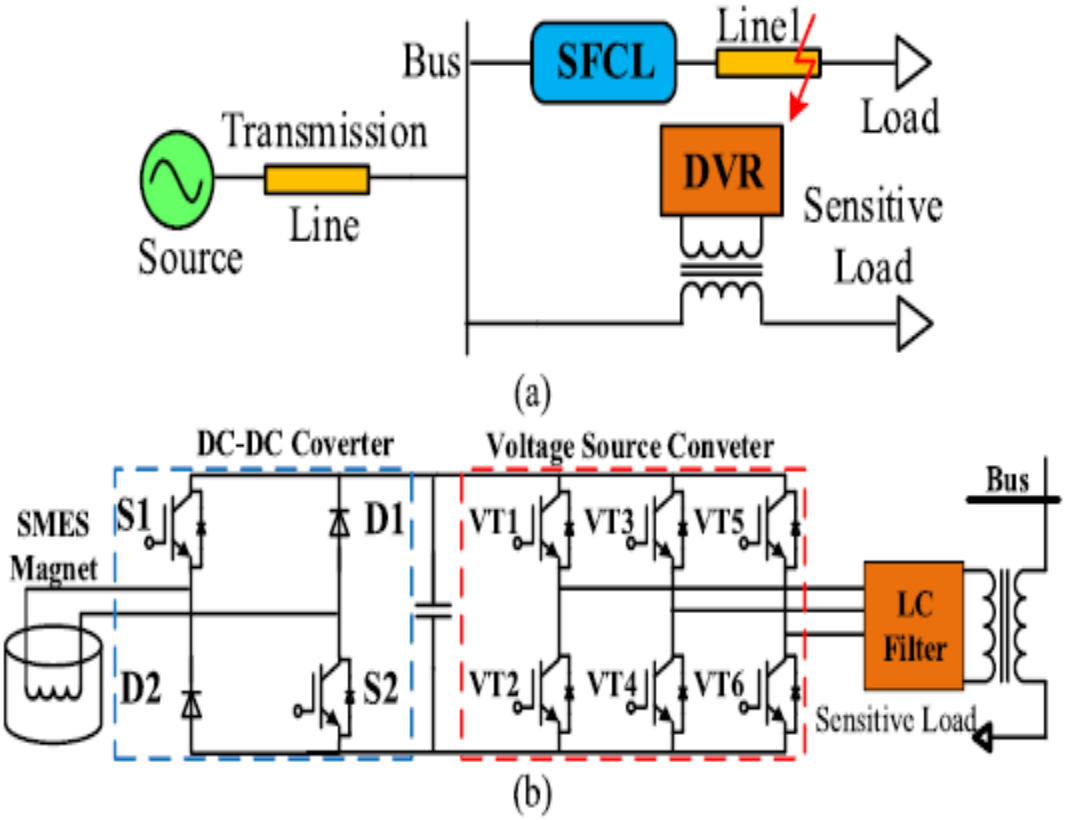


Fig.1(a) SMES-based DVR and SFCL system topology. (b) the SMES-based DVR comprehensive topology

III. SYSTEM PRINCIPLE AND CONTROL STRATEGY

SMES-based DVR Control Strategy

The DVR control strategy based on SMES is illustrated in the figure.2 For a DC-DC converter, the dc voltage control system is used. A bug is transferred between dc voltage relationship and the actual value to a hysteresis buffer for PWM signal to drive the two switches (S1, S2) By checking onbound status of two buttons, you can fix the dc voltage to SMES by continuously disconnecting the load mode (S1 ON, S2 ON) and discharging mode (S1 OFF, S2OFF). The excessive magnet current should be emphasized that SMES does not ensure routine work. A maximum control panel is thus equipped with the voltage change dc and the current limit of the SMES magnet.

ISSN- 2394-5125 VOL 7, ISSUE 04, 2020

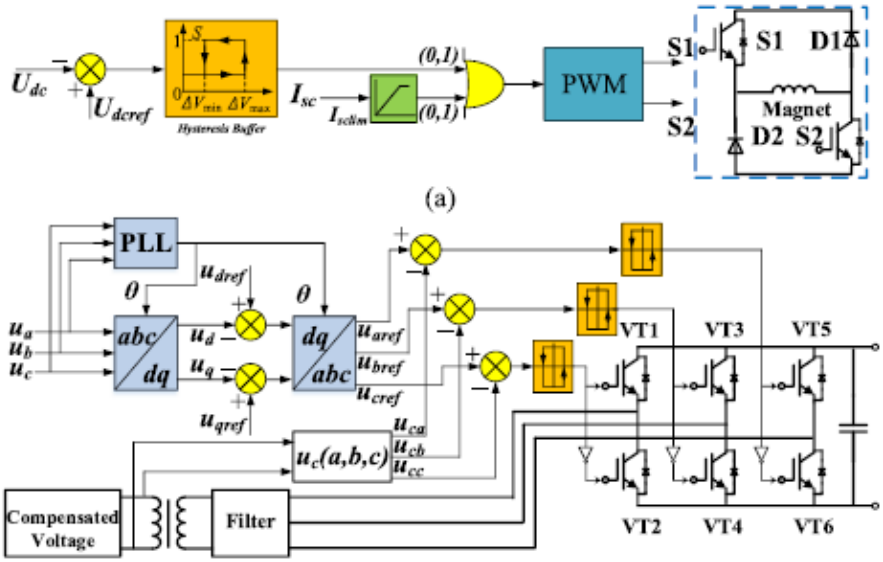


Fig.2 (a) The DC-DC converter's dc voltage control technique. (b) VSC 's strategic pre-sag compensation.

However, as shown in the fig.2(b), a pre-sag compensation plan with the dq transforms for VSC control[13].The magnitude of the stable voltage is locked and stored separately, and the phase angle of the responsive load voltage is used for exacting the compensation of the voltage perturbation based on the theory of instant reaction power and the method of hysterical regulation of the voltage. The Pre-sag leads to lowest voltage of transient waveform distortion, in comparison to other strategies, such as in-phased or optimized energy recompense.

Equivalent Resistance Modeling of SFCL

In our previous study, we studied the resistive characteristic of SFCL, which suggested that SFCL performs a particular characteristic of physical condition and resistance under different currents. In addition, the SFCL resistance value, as shown in the figure, It can be split into five segments of operation shown in fig.3. The resistance curve displayed infix mathematical form. Three can be expressed by (1) or defined in all parameters.

$$R_{sfcl} = \begin{cases} 0 & t < t_s \\ SE_c I_r^{n-1}/I_c^n & t_s < t < t_1 \\ R_m & t_1 < t < t_e \\ R_m e^{-(t-t_e)/\tau_2} & t_e < t < t_2 \\ 0 & t > t_2 \end{cases} \qquad (1)$$

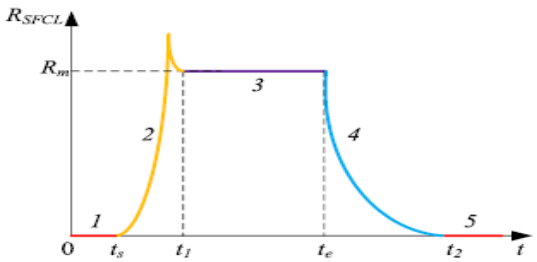


Fig. 3 SFCL 's comparable resistance in different operating environments.

ISSN- 2394-5125 VOL 7, ISSUE 04, 2020

IV. PROPOSED SYSTEM

Fig. 4 displays the total UPQC and SFCL circuit topology. The UPQC mounted at the receptive load side mainly consists of two VSC's, an LC sort, a in-grid transformers, and a condenser with D-C connection. Therefore, an SFCL is related to other feeders in sequence. The voltage-sag suppressions pro responsive load are mostly triggered by SFCL 's cooperative activity. In case of a three phase failure in a feeder that doesn't supply the responsive load, the SFCL reduces the defect current and raises the typical bus voltage slightly. On identification of a voltage-sag, UPQC is enabled in arrange to provide a compensated voltage, thereby keeping the responsive load end voltage steady.

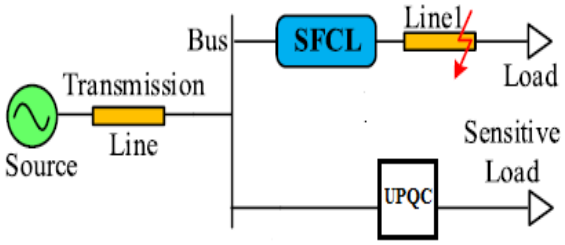


Fig. 4 UPQC and SFCL system topology

V. SMES and SFCL STRUCH PARAMETERS

A. SMES Magnetic Model

Allowing for that when it is combined with a resistive SFCL system, the necessity of temporary Upper-performance With a very high critical current SMES magnet, energy exchange operations with Smes should be anticipated. A step-mode SMES magnet with an inductance of 1.2 H and a critical current of 880 A is employed in this work. A step-shaped magnet SMES has neither end nor end nine step-shaped pancakes. The medium mount is composed of 10 serial buckets, each with 50 spindles wounded. It has 250 mm and 285 mm of inner and outer radii. Four symmetric units on both sides are made of five standard pancakes from every end of each spindle Create a cross-sectional sliding shape to the middle part. There is an internal radius of 271 mm, 278 mm, 257 mm and 264 mm. In this study , four stepped phases are associated to fulfill the enhanced demands of SMES using serial-parallel communication.This SMES combination magnet uses a minimum of around 21 km of tape.

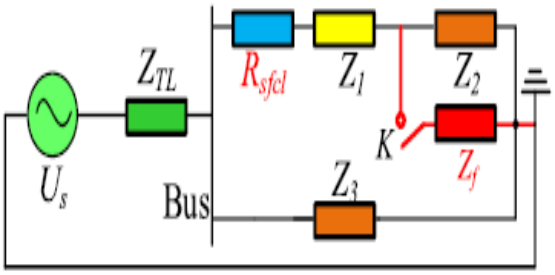


Fig. 5. The distribution system comparable circuit.

ISSN- 2394-5125 VOL 7, ISSUE 04, 2020

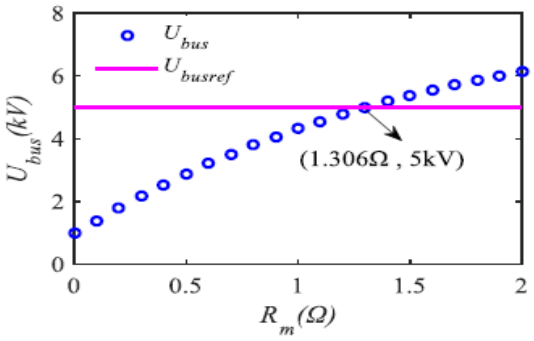


Figure. 6 The relation curve between *Rm* and *U*bus .

B. Resistance Estimation of SFCL

Figure 1(a) displays the corresponding circuit of the delivery network. For a fault of three steps, the switch K closes, the bus voltage is expressed via a single supply.

$$U_{\text{bus}} = \frac{Z_I}{Z_{tl}(Z_I + Z_3) + Z_I Z_3} U_s \qquad (2)$$

where,

$$Z_I = R_m + Z_1 + \frac{Z_2 + Z_f}{Z_2 Z_f} \qquad (3)$$

Where Ztlis is the total transmission line impedance; where Rm is a steady SFCL resistance; where Ztlis is an initial line point from a fault position; Where Ztlis is from the end of the load impedance and the same impedance to the fault position; where Ztlis is a responsive load impedance.

Equations (2) suggest an SFCL Rm-dependent bus voltage (Ubus).Therefore, based on (2), the SFCL resistance can be calculated to fulfill the required bus voltage. As shown in Figure, the relationship curve between Ubus and Rm can be achieved. 5. It shows that the SFCL strength of 1.306 is set for the common bus voltage to be increased to 5 kV (0.5 up).

VI. SIMULATION RESULTS

EXSITNG RESULTS

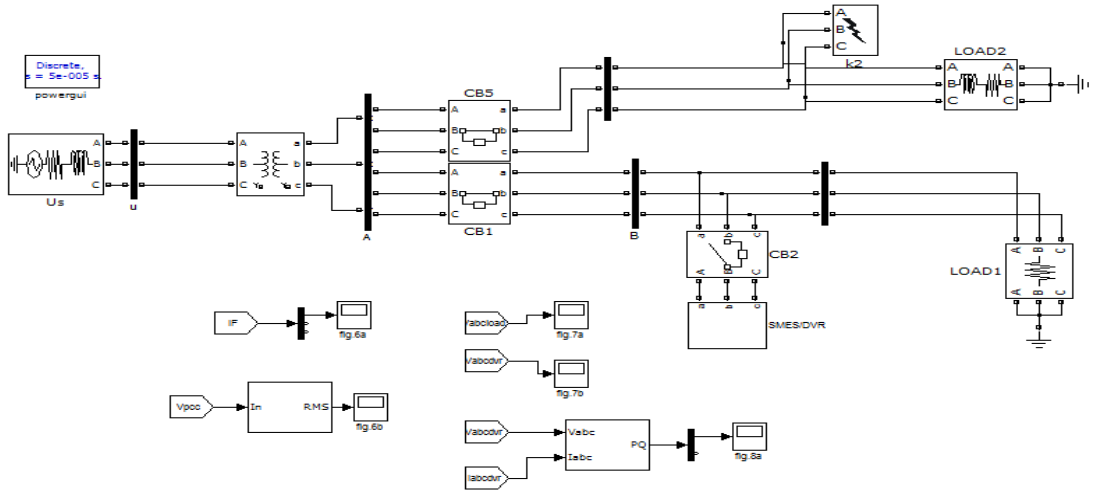


Fig 7 MATLAB/SIMULINK circuit diagram of the SMES-based DVR and Without SFCL

ISSN- 2394-5125 VOL 7, ISSUE 04, 2020

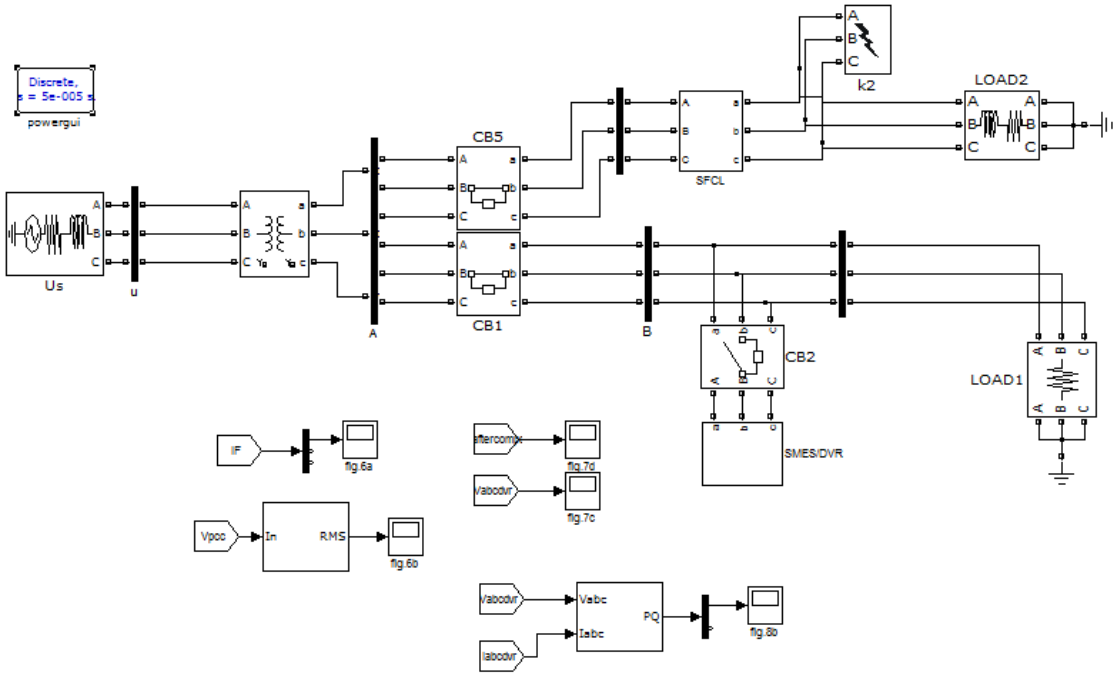


Fig 8 SIMULINK/ MATLAB circuit diagram of the SMES-based SFCL and DVR

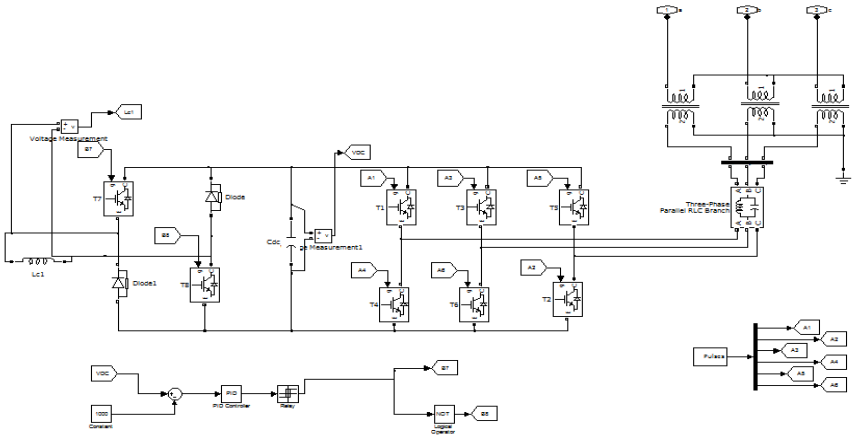
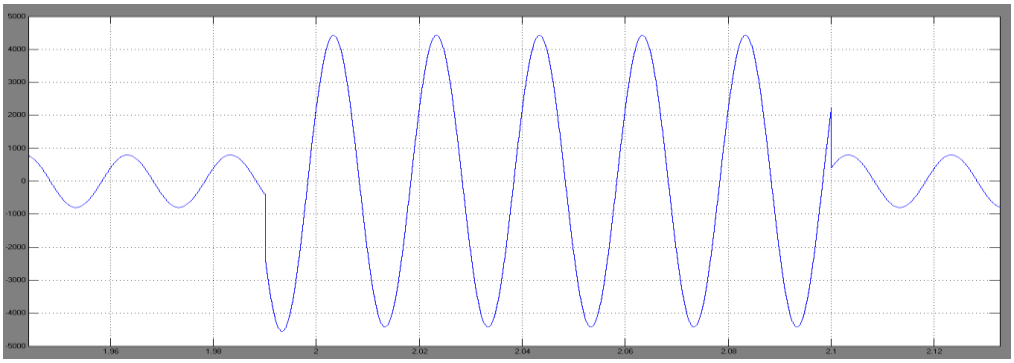


Fig 9 SMES-based DVR info topology

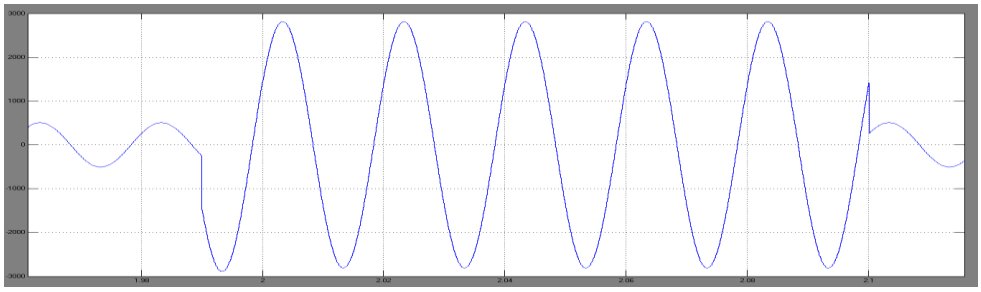
Voltage Compensation Performance with DVR and With DVR & SFCL

Fig. 10 and 11 suggest a fault current with two stress compensation schemes on distribution line 1. The original peak fault current value is decreased to 2.86 kA for the cooperative scheme that combines SFCL and DVR (SFCL&DVR). This is less than that for the single fault value method (4.50 kA). The constant fault current (with single DVR) is also limited to 2,78 kA (with DVR +SFCL) and 4,09 kA. The bus tension from 1.0 kV, as shown in the Figure, is also increasing to 5.0 kV (with SFCL&DVR. (b) 6(b). Thanks to the suppression of the fault current, the voltage loss of the transmission line is high. This is therefore assumed that, because of its high strength during distribution line fault, the SFCL not only prevents the malfunction current effectively but raises the normal bus voltage.

ISSN- 2394-5125 VOL 7, ISSUE 04, 2020

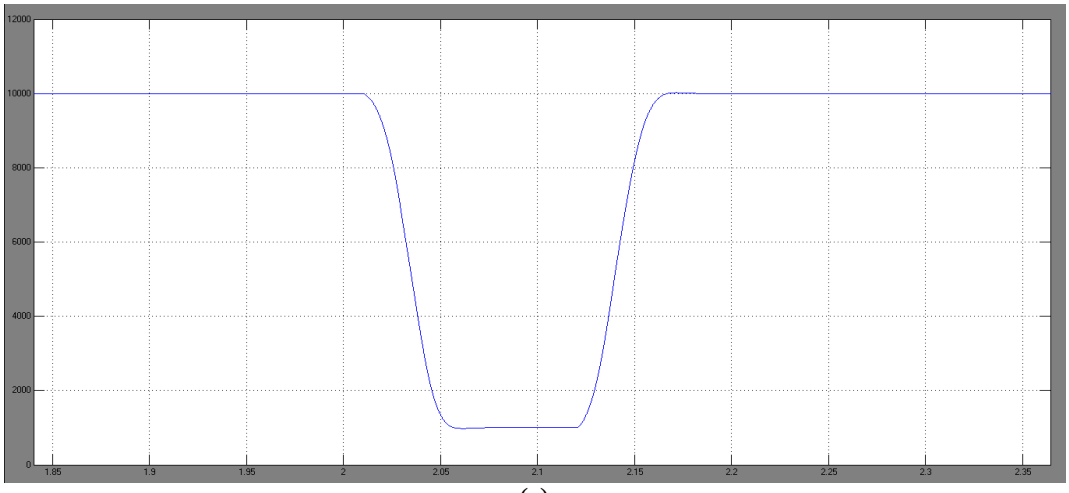


(a)



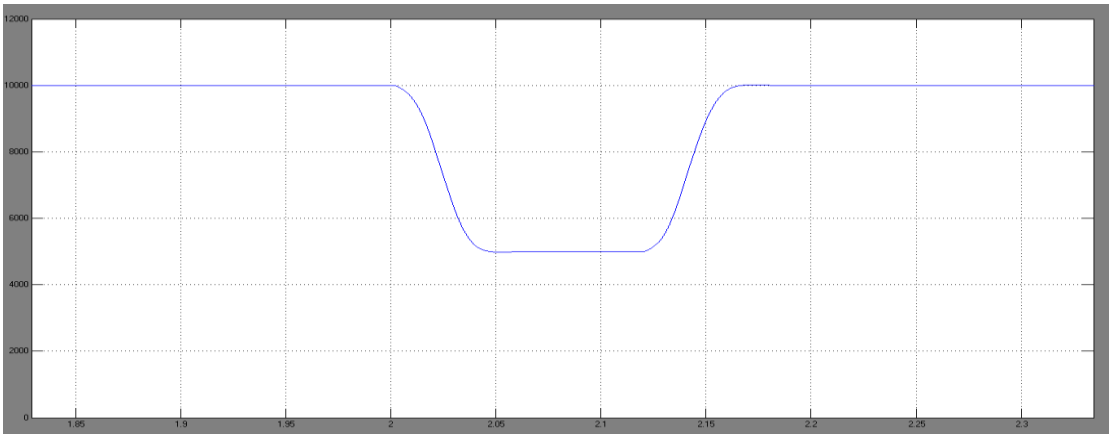
(b)

Fig. 10 (a) distribution line1 failure current with a DVR only and (b) distribution line1 failure current with SFCL&DVR



(a)

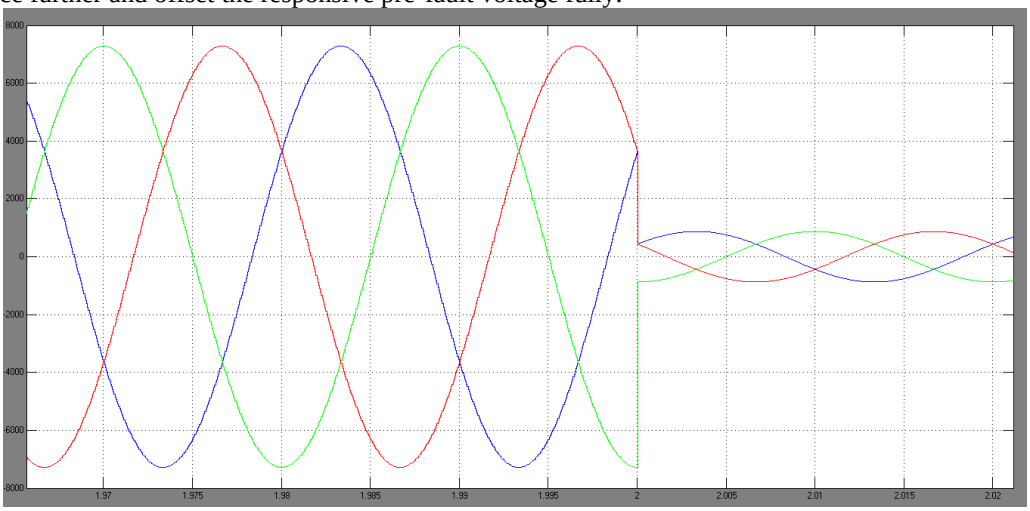
ISSN- 2394-5125 VOL 7, ISSUE 04, 2020



(b)

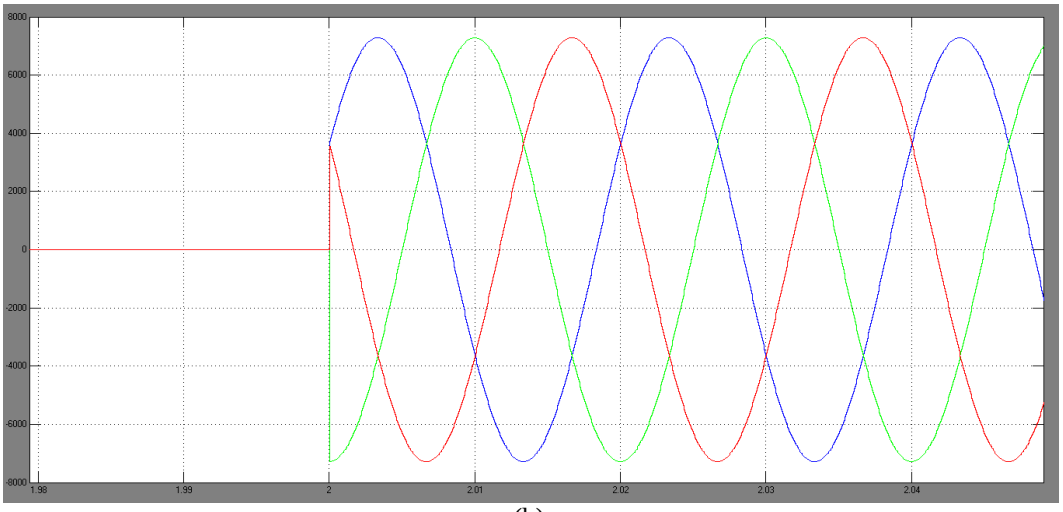
Fig 11 (a) The normal rms voltage with DVR and (b) SFCL&DVR common bus rms voltage.

The responsive weight end voltage and a DVR output voltage are illustrated in the figure. 12. Fig. 12(a). 12(d), it has been apparent from both of these DVR SFCL&DVR models that the sensitive load voltage can be completely increased to the pre-fault value within 8 ms and thus the negative voltage effect on the sensitive load can effectively be eliminated. However, The DVR voltage is only roughly 4.15kV as the additional SFCL bus voltage is raised in the suggested SFCL&DVR system, while the proposed SFCL&DVR system in one DVR system is up to 7.3kV. The proposed SFCL&DVR scheme could therefore also reduce the compensated voltage required for DVR, reduce DVR performance further and offset the responsive pre-fault voltage fully.



(a)

ISSN- 2394-5125 VOL 7, ISSUE 04, 2020



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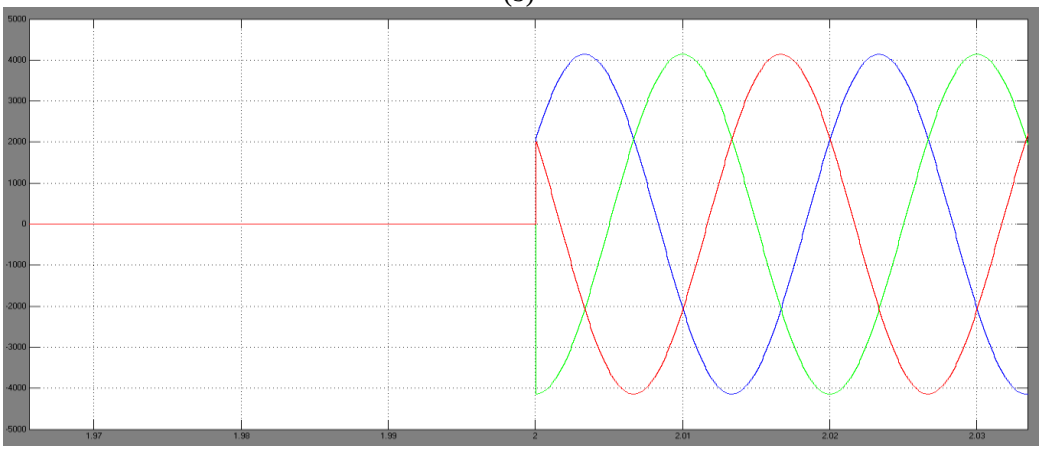
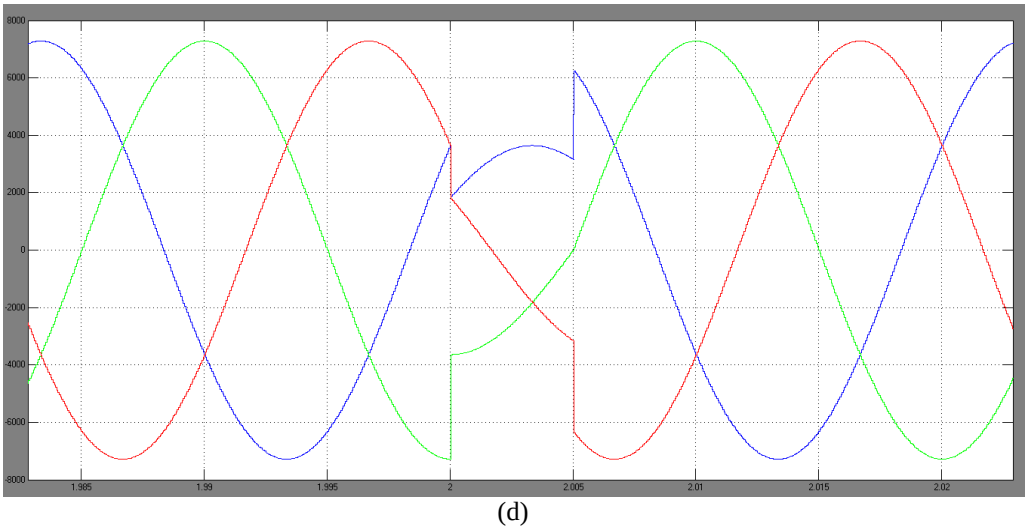


(c)



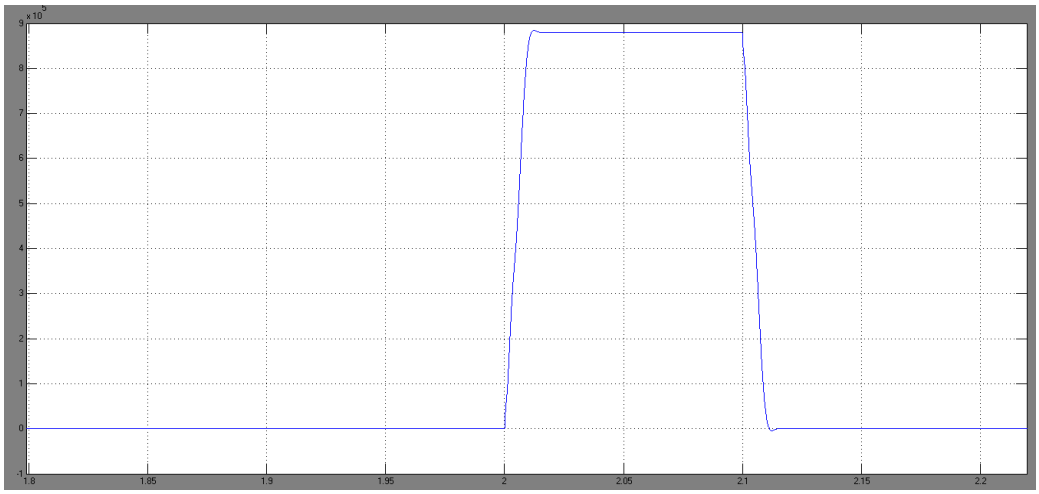
(d)

Fig. 12 (a) The load voltage, without compensation, is sensitive. (b) DVR single output tension. (c) output voltage of SFCL&DVR DVR. (d) Sensitive load voltage compensation.

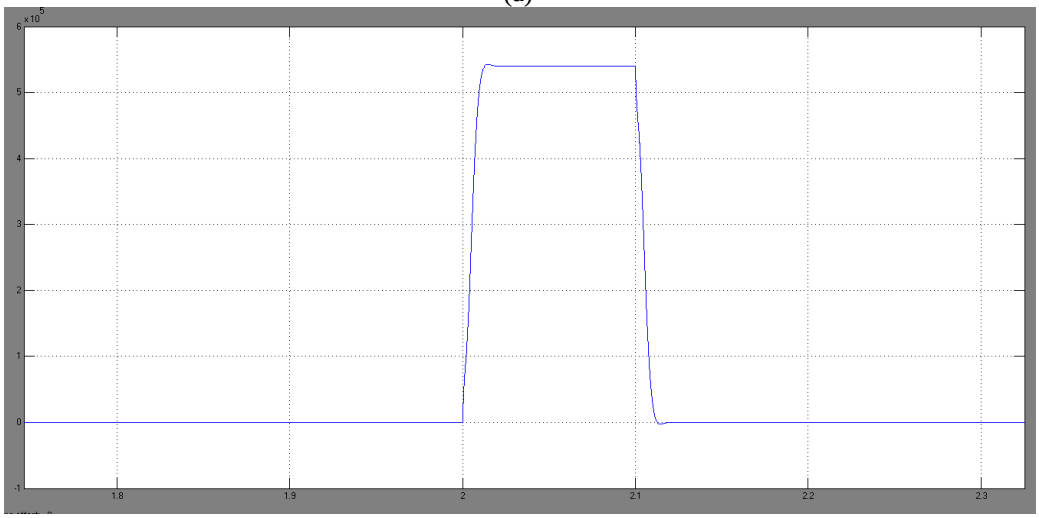
ISSN- 2394-5125 VOL 7, ISSUE 04, 2020

Evaluation of results and DVR relation

Fig. 13 Displays DVR power compensated output by two compensation systems. With the SFCL&DVR system suggested, DVR's compensated output power decreases to 0.54MW, 1.63 times the power of single (0.88 MW) DVR. Thanks to the voltage improvement effect of the common bus for common bus, the additional SFCL will effectively minimize the voltage drop of the common bus depth and thereby minimize DVR's compensated electrical power demand to reduce capital costs.



(a)



(b)

Fig. 13 (a) Compensated efficiency of single DVR and DVR control (b) Output compensated power of SFCL&DVR

ISSN- 2394-5125 VOL 7, ISSUE 04, 2020

EXTENSION RESULTS

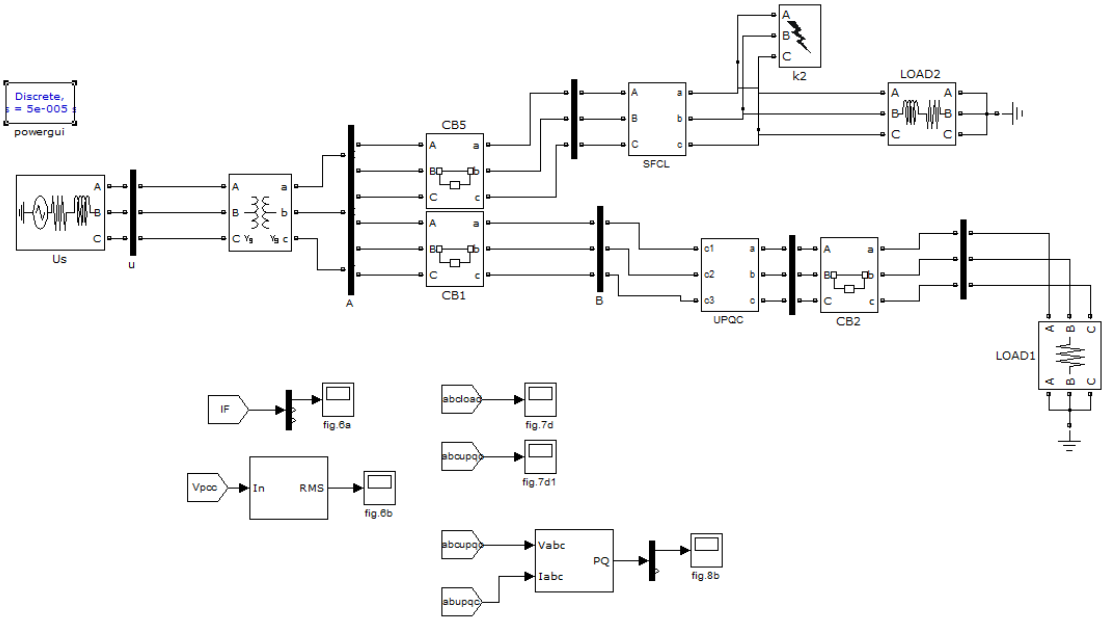


Fig 14 UPQC circuit chart with SFCL MATLAB / SIMULINK

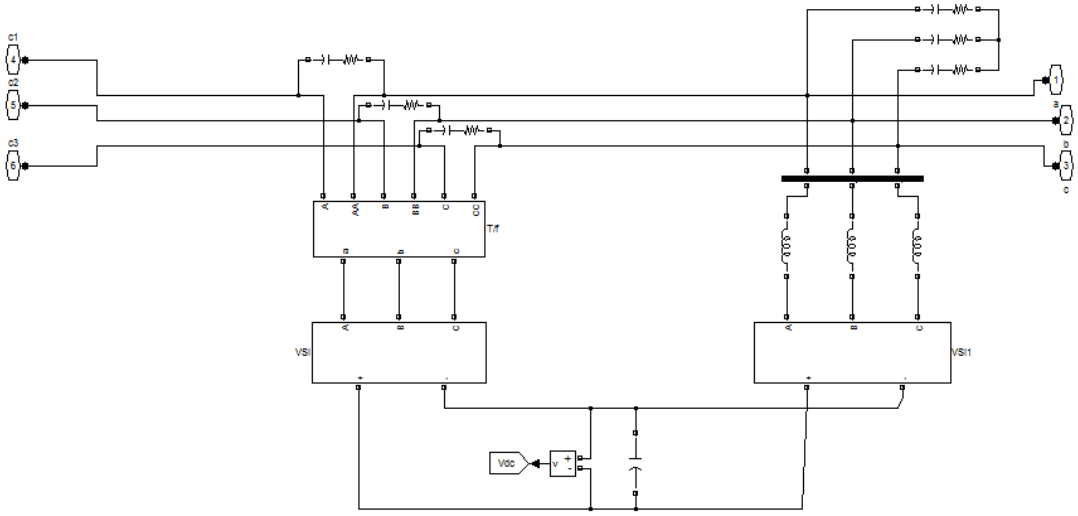


Fig 15 UPQC subsystem

ISSN- 2394-5125 VOL 7, ISSUE 04, 2020

Voltage Compensation Performance with SFCL & UPQC

The distribution line 1 error current with the voltage compensation scheme is shown in 16 and 17. In the context of the proposed cooperative system involving SFCL and UPQC (SFCL&UPQC), the original value of the defective current (initial peak value) is lower than the SFCL&DVR (2.86 KA).Similarly, the steady failure current (with SFCL&DVR) is limited to 1,74 kA (with SFCL&UPQC) from 2,78 kA. In addition, the autobus voltage (with SFCL&DVR) is augmented from 5,0 kV to 8,0 kV (including SFCL&UPQC). 7.05. Thanks to the suppression of a error present, the voltage loss of the transmission line is high. This is therefore assumed that, because The SFCL not only stops the unstable current efficiently, it also raises the normal bus voltage because of its high intensity during a breakdown on a distribution line.

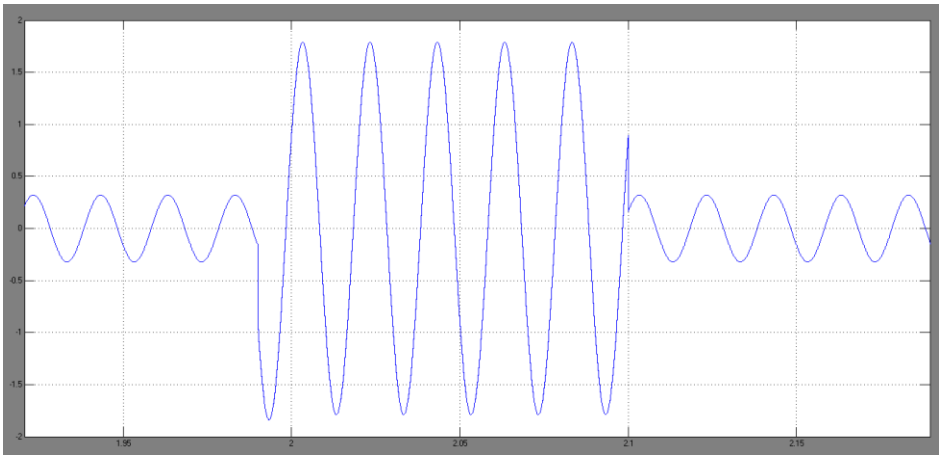


Fig 16 Present fault on SFCL&UPQC distribution line1

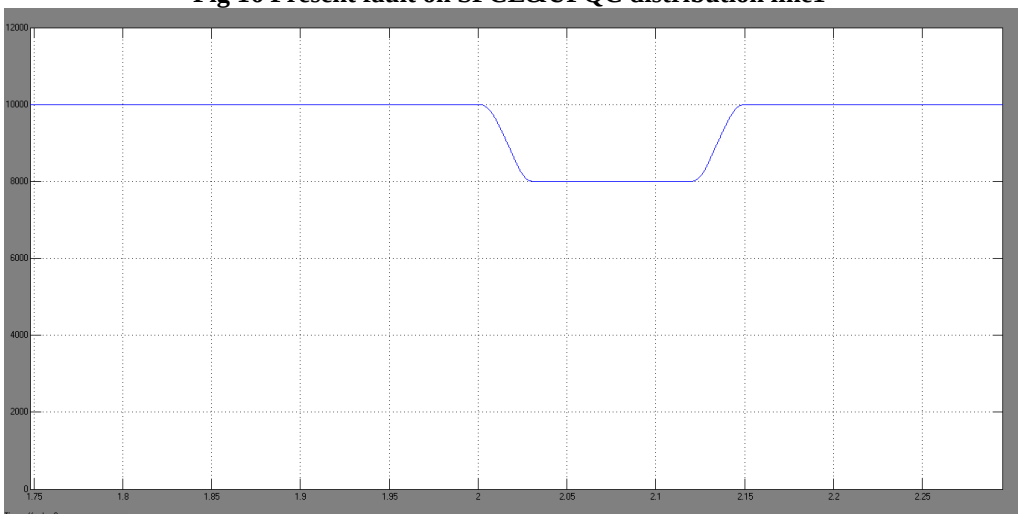


Fig 17 Common bus RMS voltage with proposed SFCL& UPQC

When looking at figures 18 and 19, it is obvious that the sensitive load voltage can be increased by both SFCL&DVR and SFCL&UPQC within approximately 8 meters to a pre-default value, reducing the adverse voltage effect on sensitive load. The additional voltage rise in the popular SFCL bus also means that the UPQC output voltage in this SFCL&UPQC scheme is approximately 3.2kV only, while the UPQC output voltage in the SFCL&DVR scheme will be increased to 4.15kV. The proposal for SFCL&UPQC that also reduce the compensated voltage requirement of SFCL&DVR, and further reduce the efficiency of SFCL&DVR while completely offsetting the pre-fault value of the responsive load voltage.

ISSN- 2394-5125 VOL 7, ISSUE 04, 2020

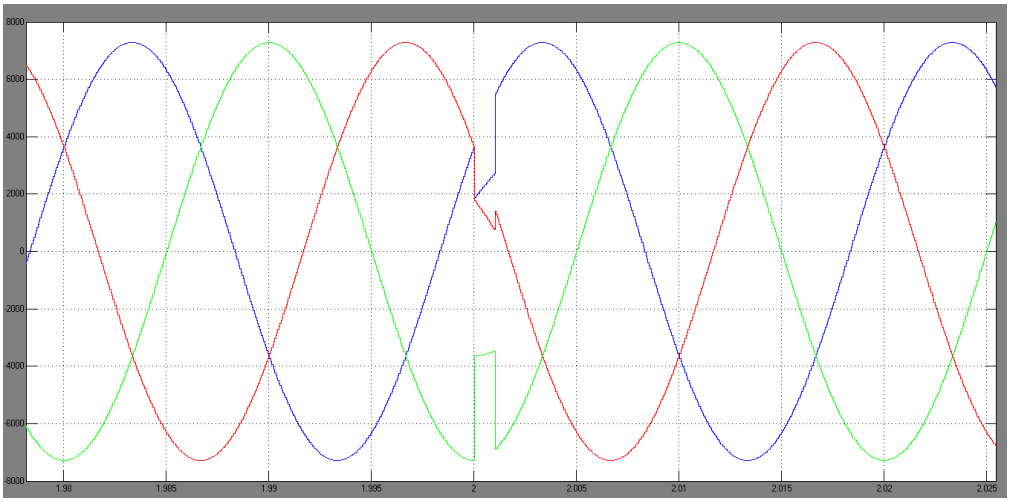


Fig 18 UPQC output voltage with SFCL&UPQC

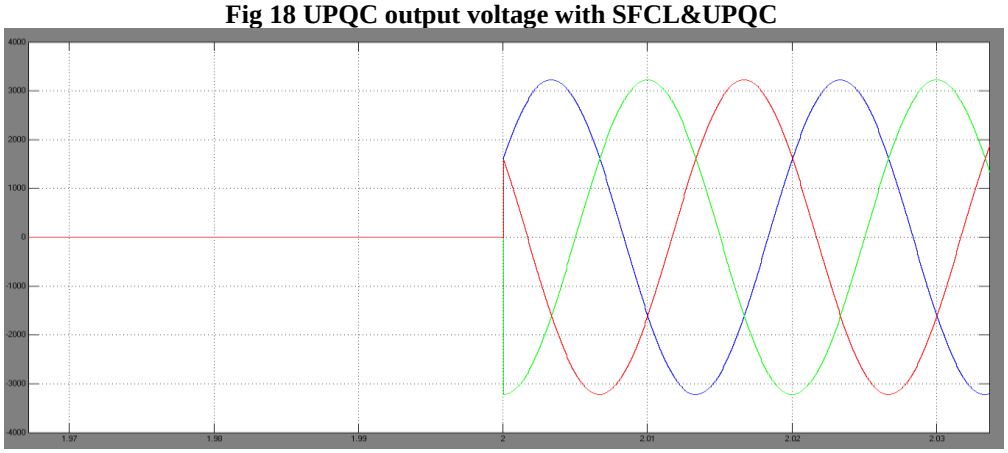


Fig 19 Sensitive load voltage with compensation

Performance Evaluation and Comparison of SFCL&DVR

Fig. 20 shows the output power compensation scheme for UPQC. With the new SFCL&UPQC system, the performance compensated power of SFCL & DVR has dropped to 0.33MW, 1.15 times lower than the power compensated in the SFCL&DVR (0.54 MW) system. The additional SFCL will decrease the voltage depth of the standard bus due the voltage increase for the standard bus.

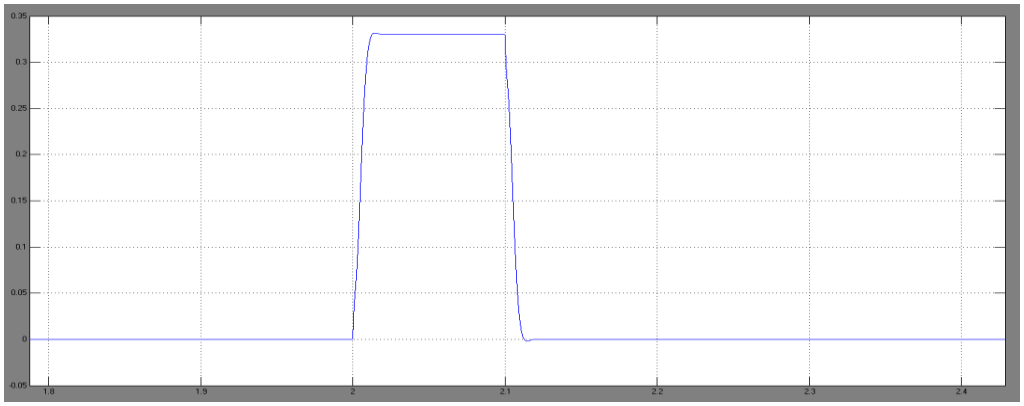


Fig 20 Input offset capacity of SFCL&UPQC proposed

ISSN- 2394-5125 VOL 7, ISSUE 04, 2020

VII. CONCLUSION

The proposed and demonstrated voltage sag- compensation scheme is base on a SFCL UPQC system. Clear discussion of conceptual design, compensation theory, control method, measurement criteria, simulation outcomes and performance assessment will take place. With a pre-sag compensating strategy the proposed SFCL&UPQC system is capable of maintaining a pre-fault value of the vulnerable load voltage During the regular bus stress. Not only does the additional SFCL suppress error energy effectively, but the usual bus voltage also increases due to its high power. More important than the SFCL&DVR, it is evident that, due to the effect of the SFCL voltage increase for the common coach, the SFCL&DVR capacity requirement might be reduced by the proposed SFCL&UPQC regime. This could further reduce the total capital cost for the SFCL&DVR. The UPQC-based SFCL is therefore intended to use in the current distribution power network to increase transient voltage efficiency.

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