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ANALYSIS ON MEMORY WITH BiCS DFT MODEL USING LEAKAGE TECHNIQUES

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ABSTRACT

BiCS technology is one of the strongest candidates for future ultra-high density three-dimensional memories to overcome problems with memory cell decline due to limited lithography technology and achieve an ongoing bit cost reduction. P-BiCS Flash is designed to solve critical BiCS Flash problems like poor memory reliability, reduced select gate cut-off and high source line resistance. This paper provides a new approach to State space generation for dynamic fault trees and a method for synthesis failure rates for DFTs. In 2007, we proposed a Bit Costs Scalable (BICS), which reduces bit costs by placing vertical storage punch and plug processes as a 3-dimensional memory for future ultra-high-density storage devices. It was used on NAND Flash only, the memory of BiCS Flash, and mass production technology has been established. In addition, BiCS technology can be applied to various memories. This review paper has focused mainly on the concept of the analysis of various athors proposed on the topic of BiCS DFT model using Leakage technique.

Key words: BiCS, DFT, Leakage technique.

1. INTRODUCTION

1.1 General study

The largest area block in modern ICs comprises memory. In addition, memories, including difficult and soft (transient) failures, are sensitive to failures rather than logic. Therefore, recalling the major failures in modern ICs is the most important cause of reliability. Particle impacts that cause soft errors, known as SEUs, are one of the main reasons for decreased reliability (single event upsets). This issue is confined to environmentally hostile to radiation, such as in space with previous technologies. But aggressive device size and power supply decreases with very deep submicron (VDSM) technology have severely affected the circuit sensitivity by Aggressively reducing the memory cell's critical charge.

Low-energy particles can change memory cells and make them sensitive to neutrons and alpha particles found by unstable isotopes in a chip's material. Even on the ground soft mistakes are a concern today, at least when reliability is an important feature. Error corrector (ECC) codes are often used to detect SEUs and correct them in order to keep them safe.

ECCs can, however, lead to major penalties for area, performance and power dissipation. ECC also detects and corrects only error when reading and not when the defective word occurs. In larger storage systems, the ECC error sensing and correction capabilities which may result in the

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accumulation of SEUs may be invalidated by a long delay between SEU events and error corrections. To address these inconveniences, an asynchronously constructed current sensor was used on the vertical power lines for a memory and parity bit in current sensor(BICS).

The BICS is asynchronous as particle strikes occur randomly. This makes designing the BICS more complicated to identify permanent defects than proposed synchronous BICSs. In the case of particles in the hit, the BICS placed on power lines that feed the cell detects abnormal current dissipation and locates the defective column. The parity bit allows you to locate the defective word and fix the error. The latency of error detection is deleted as SEUs are detected when this happens. The overhead area for the ECC is also significantly reduced (because for every two storage columns we use the single parity bit per memory word and a single BICS). Furthermore, read data on every reading cycle must not be checked. The read data must not be checked. A BICS is induced to decrease the voltage of a 300mV on Vdd and 400mV on Gnd Lines.

The sensor has been designed with old technology; voltage, temperature, process and current pulses have not been validated for different purposes. This will propose the new BICS, which will function reliably under high voltage, temperature, change in process and stringent noise conditions and which is designed for the current CMOS process (100nm). Simultaneously, the new BICS also dispenses less power than the last. The voltage drop induced by the new BICS is 7.5mV, and on the Vdd and Gnd line it is 8.5mV, respectively. Therefore the new BICS will not affect the noise margins of the old one.

1.2 Memory tests

The scannered design replaces most of the storage elements on a chip. These scan cells have a larger area of storage than normal ones. In a muxed scan design, the majority of scan cells are also accompanied by a multiplexer. Any roads that pass through such cells will be delayed more. If critical timing paths pass over storage elements, these elements will not be replaced by scan cells. Since most critical chip paths are passed through memory arrays, scan cells cannot replace the cells of the memory arrays. It would also be unacceptable to increase the chip zone and the power consumption by replacing memory cells with scan cells.

Since the memory cells act as non-scan storage elements and are not part of a scanning chain, memory cell transitions cannot be easily initiated and any captured values are not observed in the memory. Different techniques for testing memory arrays were developed.

1.3 Objectives

- Detection of soft error in Memory cell by using additional circuit advance BiCS in standby and operating mode(read mode)
- Memory retention analysis in Memory with BiCS DFT Model
- Efficiency analysis of memory architectures with leakage techniques.
- To present miniature design of memory using Leakage techniques.

ISSN- 2394-5125 VOL 7, ISSUE 12 , 2020

2. LITRATURE REVIEW

2.1 General study

Narrow timing margins produce delayed defects that are difficult to detect in modern digital integrated circuits (ICs). These defects become common as IC characteristics become narrower, process variations are increasing and operating frequencies are becoming more frequent. Although delay defects are not enabled at low speeds, timing failures at rated speed may result. Delay tests detect a time failure which causes defects, to ensure a circuit complies with the desired time requirements. The increase in mixed signal applications with analogue and digital component ICs, together with technological scaling, leads to a number of approaches for testing analogue sections integrated into digital systems. Detection and diagnosis a failure is an integral part of integrated circuit manufacturing because an unexpected system performance and often complete system failure can be caused by a single critical circuit failure. The need for efficient and efficient fault sensing methods provides the conditions for increasing reliability, reducing maintenance activities and cost. As the systems are increasingly complex and highly automated. A brief note is published in this review paper with several authors about analogue testing methods.

2.2 Review of Literature

Sneha Deshmukh, et.al, 2018, [1], This paper undertakes an extensive quantitative survey to simulate various predominant leakages. We analysed the DG devices for modelling the leaks in the 6T SRAM cell in detail. Our study shows that the use of DG sleep-transistor devices can significantly reduce leakage components and make the construction of SRAM cells very efficient. Though DG devices have a higher threshold voltage, the subthreshold current can decrease effectively. Gate-to-Channel leakage is also reduced because there is no bulk charge for DG.

Amit Saxena, et.al, 2016, [2], This paper has shown a new application of the adiabatic switching principle to the SRAM design that can be implemented without increasing the complexity of the area or the circuit. Our design offers the flexibility to optimise the SRAM from architectural aspects as a whole. Results suggest that SRAM offers the basic benefit of adiabatic logic, that of low-power.

Jeong Beom Kim, et.al, 2014, [3], The quiet current supply monitoring, also known as I DDQ testing, has recently received considerable attention.

ISSN- 2394-5125 VOL 7, ISSUE 12 , 2020

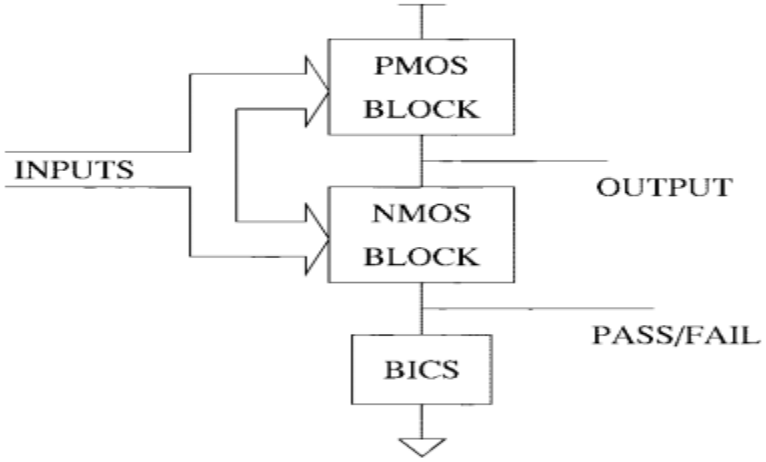


Fig. 1. IDDQ testing block diagram.

Fig. 1 shows a general I DDQ internal test structure for inserting the BICS from the CUT to the GND. BICS checks if the quiet current has a level less than or higher in an integrated circuit. Our BICS detects an abnormal current due to constant production defects in test mode. In addition, neither an external voltage reference nor a power source is required for the BICS. The BICS therefore needs less space and is more efficient than standard current sensors.

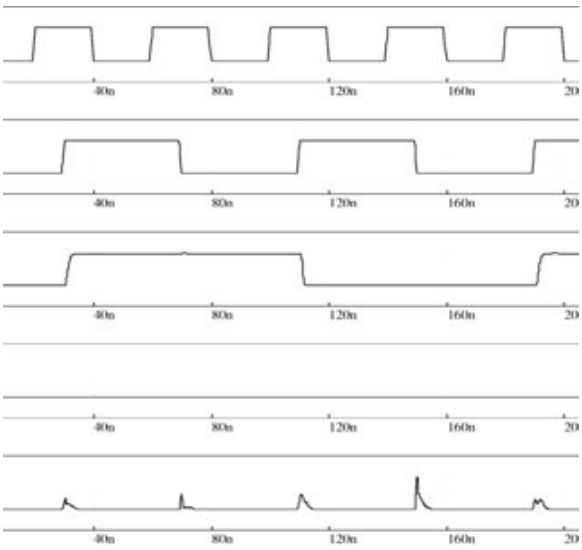


Fig 1.1: Simulation of a defect-free test chip without BICS.

The proposed BICS is simulated using HSPICE BSIM1 models on a SUN SPARC server 1000. The simulation result without BICS is shown Fig. 1.1.

ISSN- 2394-5125 VOL 7, ISSUE 12 , 2020

D. Sargsyan, et.al, 2018, [4], This paper presents the BIST memory firmware generation architecture. The proposed method and firmware have been applied experimentally in various automotive projects with different scenarios. In the firmware verification process the Verilog test bench with PLI support and an integrated test bench were successful in two different types of test bench generation. To control access to embedded memories and provide flexible field testing in mission modes, Synopsys STAR memory system was implemented.

L.Saranya, et.al, 2018, [5], In this paper, we design a different low power SRAM cells categorized as 6T, 8T which increases the functionality of the circuit and it has high stability in read operation and ability in write operation. The simulation is carried out by using TANNER TOOL. The purpose of this paper is to analyse the 6T SRAM static noise margin (SNM) during reading operations, using 180 nm technology to increase transistors. Using this paper, we can overcome the power consumption due to additional transistor. In this paper, we use 6T SRAM in 45nm CMOS technology to provide interface with CPU and to replace DRAMs in system. We can overcome the large fraction of total power in SRAM cell. Here, we can provide low leakage power using improved self controlled voltage level circuits in 9T SRAM which results in total average power.

Sheetal Barekar, et.al, 2020, [6], The cell design is carried out using the cell ratio and pull-up ratio to ensure readability and good writing ability. The peripheral circuits are also designed to match the designed cell. For the detection of faults at different locations in the cell, the Pre-discharged feeble cell detection method is proposed. A wide range of resistive defect values is used from 0 ohms to Tera ohm to detect the faults. With the help of Predischarged Feeble Cell Detection, the open resistive defect faults in the memory can be easily detected with improved values. The bridging defects can also be detected by using the proposed method. With the combination of multiple read cycles, the dynamic read destructive fault can be detected as well.

G.C. Medeiros, et.al, 2018, [7], This study contains an approach to test defects to detect resistive defects in FinFET memory cells by connecting OCCSs to VDD and GND. All resistive defects were detected in a certain degree, irrespective of whether causing static or dynamic defects. Compared to other March tests, the approach proposed has a very short test time. Future work includes the analysis of the impact of intercell defects.

ISSN- 2394-5125 VOL 7, ISSUE 12 , 2020

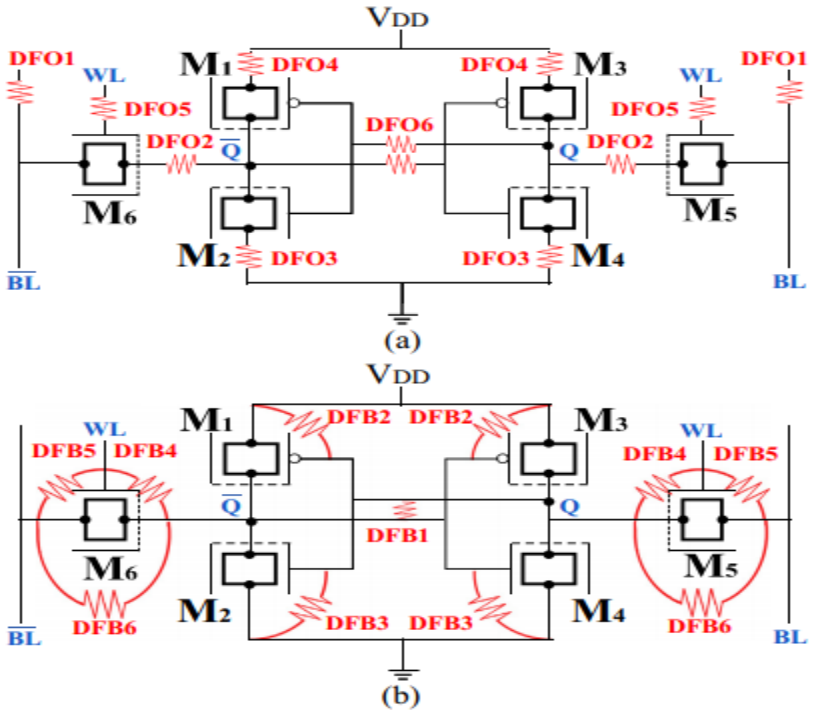


Fig. 2. Set of resistive defects injected in memory cells: (a) Resistive-Open and (b) Resistive-Bridge defects.

The 6T cell schematics including the resistive defects injected are shown in Fig. 2. The defects are designed to be resistive-open (RO), creating resistance in existing connections (fig. 1(a)) and resistive bridges (RB). These defects are modelled as resistive-open (RO).

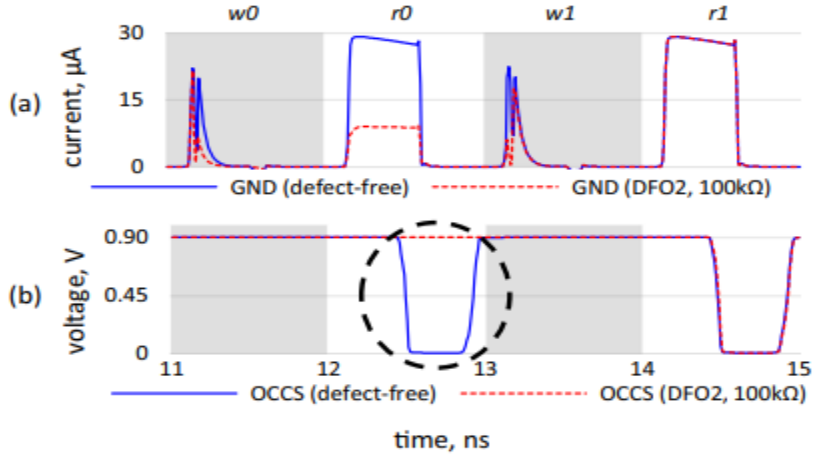
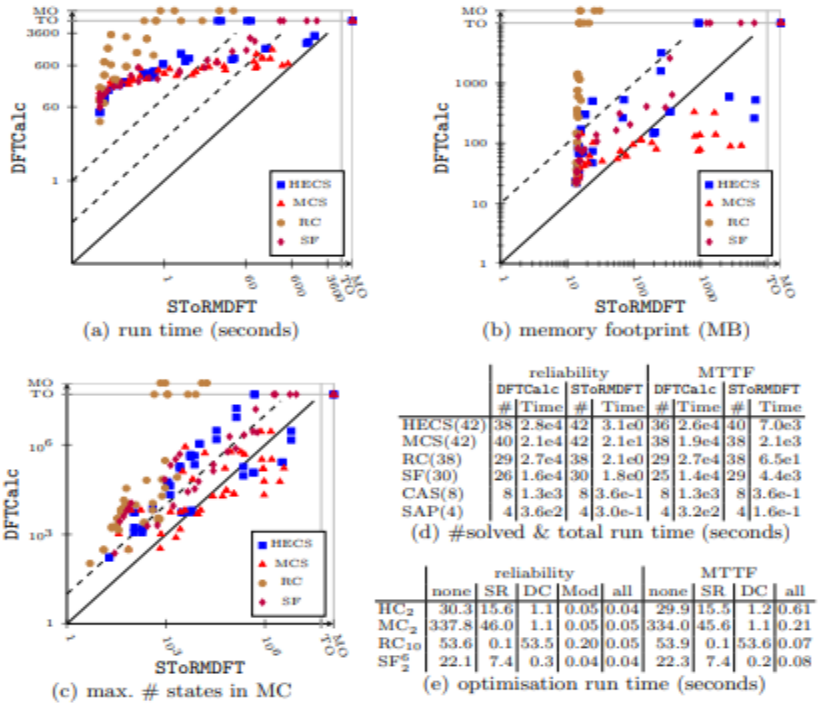


Fig. 1.2. (a) GND discrepancy caused by a resistive-open defect, and (b) the output of the OCCSs.

ISSN- 2394-5125 VOL 7, ISSUE 12 , 2020

Fig. 1.2 depicts the input and output waveforms of the OCCS detecting the DFO2 = 100 kΩ when the March element ⇓(w0, r0, w1, r1) is executed. Part a of the figure shows the input current to the OCCS that is connected to the ground, while part b the output voltage. The blue lines represent the signals for a defect-free cell, while red dashed lines represent the cell's signals for a defective cell (DFO2). During the r0 operation, there is a sharp discrepancy in current consumption between cells. This disparity results in the PWM circuit producing two distinct signals at the OCCS's output, highlighted in Fig. 1.2(b).

Matthias Volk, et.al, 2016, [8], This paper provides a new approach to state space generation for dynamic fault trees and a synthesis technique for failure rates in DFTs. The Dft structure, which detects symmetries, falsely non-deterministic ones, is exploited aggressively by our state-space generation technique. Benchmarks show an increase of more than two orders in state space generation and analysis time. With symbolic failure rates, our approach supports DFTs and complements parameter synthesis. This allows the maximum tolerable failure rate of a system component to be determined while ensuring that the intermediate failure time is below the threshold.



	reliability				MTTF			
	DFTCalc		STORMDFT		DFTCalc		STORMDFT	
	#	Time	#	Time	#	Time	#	Time
HECS(42)	38	2.8e4	42	3.1e0	36	2.6e4	40	7.0e3
MCS(42)	40	2.1e4	42	2.1e1	38	1.9e4	38	2.1e3
RC(38)	29	2.7e4	38	2.1e0	29	2.7e4	38	6.5e1
SF(30)	26	1.6e4	30	1.8e0	25	1.4e4	29	4.4e3
CAS(8)	8	1.3e3	8	3.6e-1	8	1.3e3	8	3.6e-1
SAP(4)	4	3.6e2	4	3.0e-1	4	3.2e2	4	1.6e-1

(d) #solved & total run time (seconds)

	reliability					MTTF			
	none	SR	DC	Mod	all	none	SR	DC	all
HC_2	30.3	15.6	1.1	0.05	0.04	29.9	15.5	1.2	0.61
MC_2	337.8	46.0	1.1	0.05	0.05	334.0	45.6	1.1	0.21
RC_{10}	53.6	0.1	53.5	0.20	0.05	53.9	0.1	53.6	0.07
SF_2^6	22.1	7.4	0.3	0.04	0.04	22.3	7.4	0.2	0.08

(e) optimisation run time (seconds)

Fig. 1.3. Overview of the experimental results on four different benchmark sets.

Figures 1.3(a-c) compare the performance of our tool (referred to as SToRMDFT) with DFTCalc on MTTF (where modularisation is not applicable). All plots use a log-log-scale. Fig.1.36(a) presents the analysis time of a DFT. This includes state space generation. The lower dashed line indicates an

advantage of our tool by a factor ten, the upper of a factor 100. The outer lines indicate TOs and MOs, respectively. Fig. 6(b) indicates the peak memory consumption as given by the operating system. Fig. 1.3(c) shows the peak intermediate state size. Figure 1.3(d) summarises the performance on the benchmark sets — it lists the number of benchmarks solved and the cumulative time needed for the solved benchmarks. Figure 1.3(e) shows the effect of the individual optimisation techniques (symmetry reduction, DC-propagation, modularisation) versus using all of them.

Majdi Ghadhab, et.al, 2019, [9], This paper makes two main contributions: In a potential automotive environment, we report on the use of dynamic fault trees in safety analyses. The DFT is used newer in this field, although the standard analysis of fault tree is part of ISO 26262. This paper shows how DFTs offer additional features that help to create faithful scenario models. The models are then used to analyse the scenarios in issue. We provide concrete building blocks, e.g. redundancy and faults covered under fabled security mechanisms, for an increase in the applicability of DFTs as a means to test the probabilistic safety in industrial environments.

Ezeogu Chinonso Apollos, 2019, [10], This article presents a memory design for 6T and 9T SRAM in 45nm CMOS technological node. Both designs have been assessed in terms of performance. The performance criteria included stability, power or current and process leaks, voltage and variation in temperature. The N-curve was more advantageous for stability measurements because of the advantages of data provided by the N-curve about voltage, current and power in one plot. The N-curve was also used for stability criteria. In the read margin, the 9T SRAM has been found to be more stable because the pass-gate transistors are used and the read current path isolated using transistors with minimum feature size; less leakage and power than the 6T SRAM.

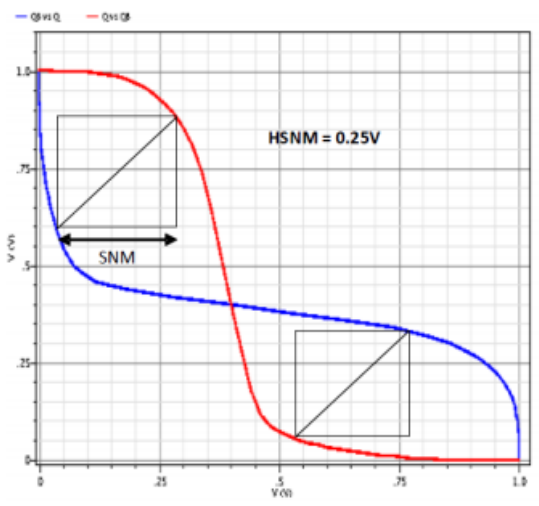


Figure 1.4. 6T and 9T Hold SNM for CR=1.5.

ISSN- 2394-5125 VOL 7, ISSUE 12 , 2020

The hold SNMs for the 6T and 9T SRAM are the same because the same symmetry of 6T SRAM design was used with additional three extra transistors to improve the read margin in the 9T SRAM design. These transistors are cut-off during hold state, therefore given an equivalent 6T SRAM configuration (see figure 1.4).

Robin Haunschild, et.al, 2016, [11], This paper provides an overview of DFT literature in total and compound terms. Total DFT literature was analysing in research subjects while combination of chemical elements and element combinations were analysed by compound-related DFT literature. In the 1990s, DFT-related literature grew exponentially. The growth of publications relating to DFT has been linear since 2000. The publication volume of DFT is currently doubling every five to six years.

BATHINI SANDHYA RANI, et.al, 2017, [12], Currently, the area in the System-on-Chip (SoC) with embedded memory is more than 90% and by 2014 it should rise to 94%. The performance and the return of integrated memories therefore dominates the performance of SOCs. However, the performance of memory production is largely limited by random defects, random pinholes, random leakage failures, significant processing and assembly errors, specific processing defects, errores, pictorial defects and other defects. We propose a new programmable MBIST algorithm which gives the flexibility of choosing March algorithm after fabrication too. Area of BIST circuit can also be reduced as compared to BIST with dedicated hardware when applied to large number of BIST algorithms.

Tang and Pun's existing FVF-based input comparator were suggested as a high speed, powerful change. The performance of the current comparator is compared to Tang and Pun when it comes to the delays in propagation, dissipation in power and PDP. The proposed current comparator was equipped with a 3-bit CM Flash ADC and 2-step, 3-bit ADC Flash. The ADC performance parameters were evaluated and are satisfactory for both initiatives.

This paper presents an idea for analogue current comparison that compares high speed and accuracy input and reference currents. The proposed circuit uses the amplification of the common gate configurations, which amplifies input current voltage variation and develops a comparative output voltage. For the final CMOS compatible output voltages, cascaded inverter steps are used. Circuit power consumption can be managed by the bias voltage of the applied gate. The comparator is developed and tested for a supply voltage of 3V with 180 nm CMOS process technology.

ISSN- 2394-5125 VOL 7, ISSUE 12 , 2020

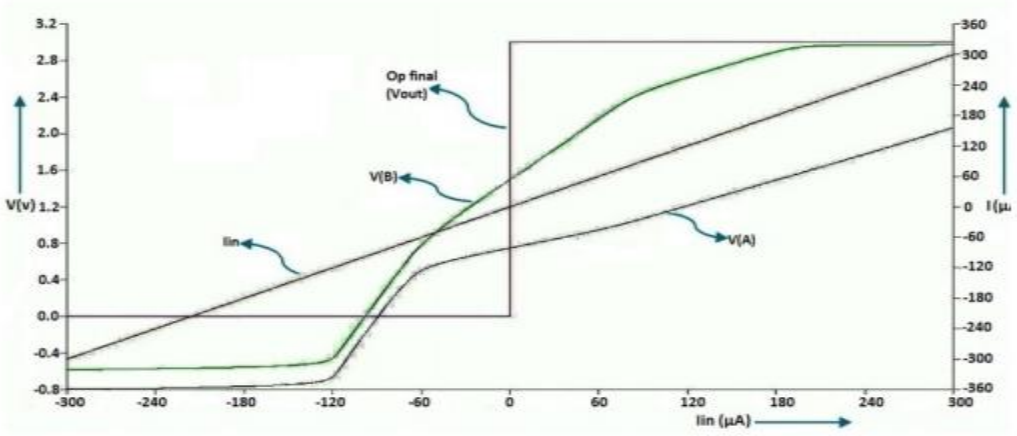


Fig.1.5 DC Transfer Characteristics.

For simulation, standard BSIM 0.18µm CMOS technology parameters have been used with 3V power supply. Circuit was designed optimally for values of speed, power and accuracy. DC transfer characteristics obtained for simulated design is shown in Fig. 1.5.

3. BICS ARCHITECTURE

This paper provides a new strategy for designing BBICSs with an optimum transient-fault sensitivity while maintaining low overheads for both areas and power. The solution enables the sensitivity of the sensor to be increased by setting an asymmetry in the voltage capacity of the sensor latch. Moreover, the BBICS sensitivity is further improven by introducing a mechanism to regulate the delay of the large-scale access transistors. The design strategy proposed offers a good compromise between sensitivity to failure detection and energy consumption and makes the use of several CMOS processes feasible.

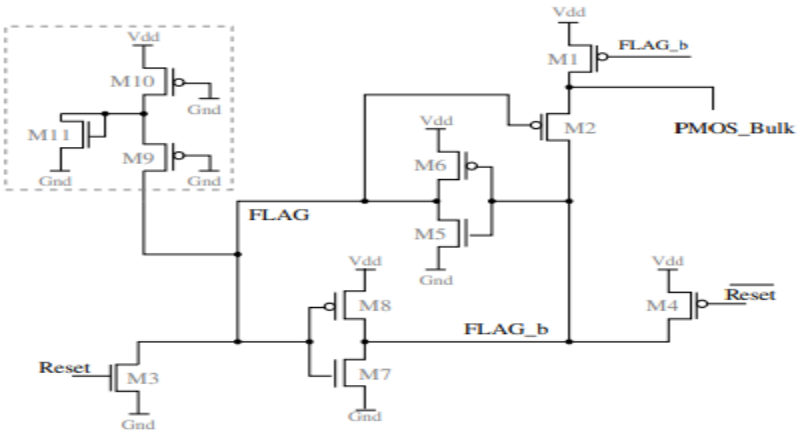


Figure 3.1: PMOS monitoring Tbulk BICS architecture.

ISSN- 2394-5125 VOL 7, ISSUE 12 , 2020

The Tbulk BICS architecture used to monitor transistors of PMOS is depicted in Fig. 3. To deal with IC variability, the Tbulk BICS uses trimmed transistors. However, for the sake of simplicity we do not analyse its effect in detail.

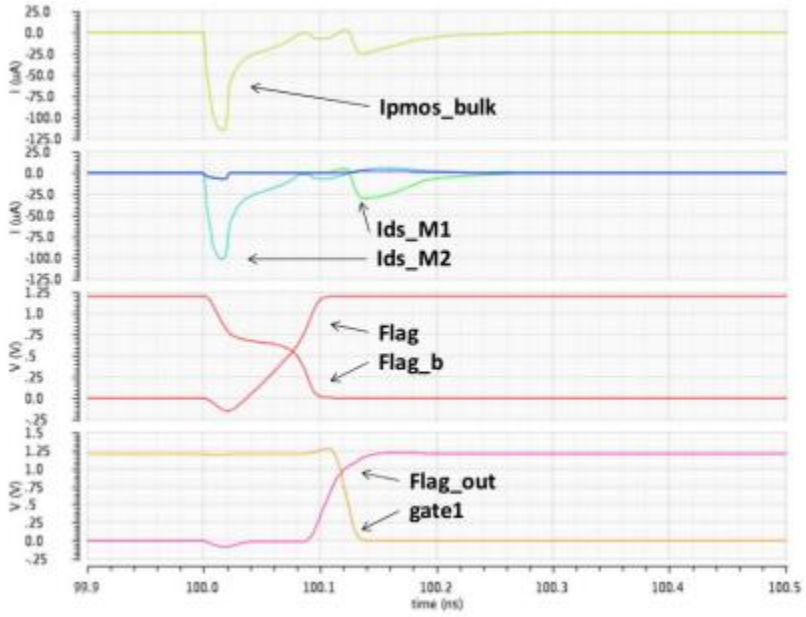


Figure 3.2: Improved pBBICS waveforms during SEE detection.

Fig. 3.2 displays the successful detection of an SEE transient current (147µA@50ps) on a PMOS of the inverters chain.

Two different 11T SRAM cell topologies with a completely selected, robust operation for the bitinterlave implementation are presented in this article. The 11T-1 and 11T-2 cells proposed the elimination of reading disturbances and the write-only '0 /'1' techniques, which would improve the writing output. 11T-1 and 11T-2 are approximately 1.83x and 1.7x and both have a read output approximately two times higher than 6T cells (VDD=0.9V). The 11T-1 cell proposed shows that the average Writing (WM) of the existing methods is 13.6 percent greater than the 11T cell. During the half selection process, the two proposed cells eliminate floating node conditions in previous interrupting cells. The Monte-Carlo simulation confirms a low-voltage operation without further peripheral assistance circuits.

ISSN- 2394-5125 VOL 7, ISSUE 12 , 2020

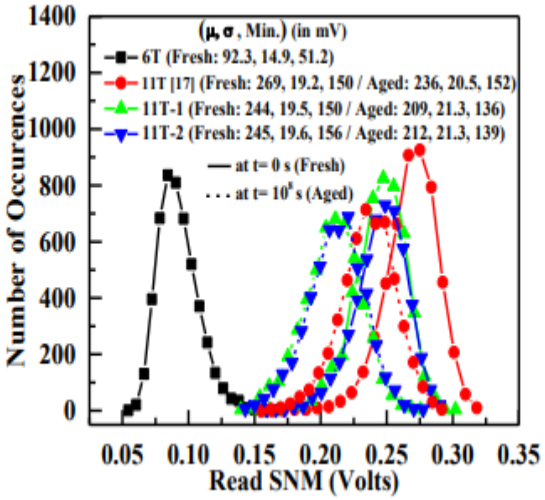


Fig. 3.3. Statistical distribution plot of RSNM for fresh and aged cell (under worst case static stress) at T=125oC and VDD = 0.9V. (6T suffers read failure due to high degradation at t=108 s).

Fig. 3.3 shows the statistical distribution of RSNM at 125oC and VDD=0.9V for the fresh as well aged cells. The 6T cell shows worst RSNM due to its conflicting sizing requirement.

This paper discusses the challenges and solutions of using built-in current sensors (BICS) for the purpose of in situ health monitoring with a safe and critical IC design. The Quiescent Current Monitor system (QCM) is developed with several BICS and digital control logics. The QCM BICS is capable of detecting a leakage rate of 4,uA, operating at system rate and having relative low overheads. A large debug capability and built-in-self testing are included in QCM digital logic (BIST). We have analogue and digital BICS analogue and embedded simulations and attached layout and tape-outs. Silicon is currently being manufactured. Results to date show that BICS can be an effective and relatively cheap way of providing the state-of-the-art health surveillance of security-critical microelectronics for certain systems.

Before using redundancy to repair memory test is necessary. The proposed design for testing techniques (DFT) in 1970, by including additional loops, improve the testability. Compared to the controlled external tester, the DFT circuit controlled via a BIST system saves more time and efficiency (ATE). However, BIST's stock memory does not deal with the loss of components due to production defects but only with screening issues. BISR technologies aim to test embedded memories, to save and replace fault addresses with redundancies. The authors suggested a new BISR memory strategy, which included two serial redundancy analysis phases (RA). Present an efficient embedded memory repair algorithm using the proposed multiple redundancies algorithm and a BISR system.

ISSN- 2394-5125 VOL 7, ISSUE 12 , 2020

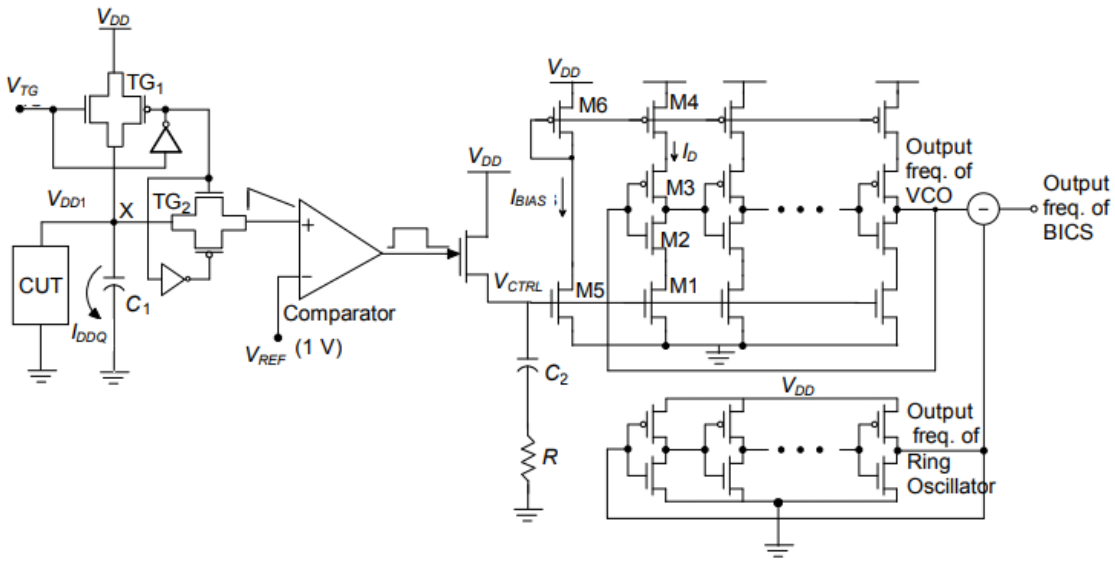


Figure 3.4. ΔIDDQ built-in current sensor (BICS).

The BICS is on-chip to improve testing and test speeds. In the design. The sensor proposed also takes into account process variation after manufacturing and automatic error detection adjustments. As an input to the NMOS switch the output of the comparator is used to charge the capacitor C2, as showed in Figure 2.

CONCLUSION

This review paper initiates an extensive quantitative survey to simulate the prevailing leakage. In addition, various authors present and compare their technological nodes with the most promising techniques for leakage reductions. More precisely, considering the effectiveness of these techniques, the impact of the development of gate tunnelling and substratum currents are studied. For the sake of need to know the more analysis on DFT models the reader is interested in considering the reviews in the area of delay test. This article also provides an evaluation of a broad range of references to DFT models, as an extensive and mature field of delay testing.

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ISSN- 2394-5125 VOL 7, ISSUE 12 , 2020

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