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Optimization of Effective Area of 3-Inputs XOR Gate Using QCA Simulation

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Abstract

Optimization of electronic circuits using Complementary Metal Oxide Semiconductor (CMOS) which is a traditional technique is going to be reaching its basic limits. An effective alternative to this CMOS technique is Quantum dot-Cellular Automata (QCA).This is so much advantageous like low power consumption, improved switching speed, reduced device size etc. XOR gate is the primary building block of most of the widely used digital circuits. Constant efforts are being made by researchers to design XOR gate using reduced number of QCA cells. In our design least number of QCA cells are used to realize the working of XOR gate which indicates lowering of power consumption, reduced area and less operation time of digital circuits based on XOR gates.

Keywords:-*QCA, 3 input XOR gate, majority gate, low power, operation time, QCA designer.*

1. Introduction

The recent era in technology is optimization of power, size and cost. In last two decades extensive researches and modification have been applied in the Very large Scale Integration (VLSI) technology using lithography based Complementary Metal Oxide Semiconductor (CMOS). But due to extensive scaling of device size, this technology is approaching fundamental physical limits. It's working almost impossible after 10nm as it can face abnormal quantum behaviour. As an alternative method Quantum dot-cellular automata (QCA) has been introduced by Craig. H. Lent around 1984.

Compared to conventional CMOS circuit, QCA is connected by quantum relations among quantum dots. These dots are not for expressing information as voltage or current, but denote digital data by the positions hold by electrons. Cell is the fundamental building block of QCA which is comprised of four dots and two numbers of electrons. Four dots positioned in a square fashion and two electrons occupy any two dots considering diagonal positions. These two diagonal positioning of electrons is termed as cell polarization. When two electrons adjust in left lower and right upper corner, it denotes state 1(+1). On the other hand when two electrons adjust in left upper and right lower corner, denotes state 0(-1). QCA technology uses cells to design digital gates. AND, OR gates are implemented using majority voter where five no of cells are connected in a cross pattern with input, output and polarized cell. NOT gate also designed using 2 or 3 cells. Design of XOR gate which is the basic building block of various useful digital circuits like adder, subtractor, multiplexer, decoder, parity generator, comparator etc, is somewhat arduous using QCA cells.

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Enormous researches have been done to design 3 input XOR gate employing minimum cells and less wire crossings. In[a] M.T .Niemier et al. has shown a QCA 'XOR' gate comprising of 60 cells, 5 gate counts, 1.5 clock latency. This design used a huge number of cells, wide area, and large time delay. As an improvement over this S. Hashemi et al. [b] has proposed 2-input XOR gate using 54 cells and 5 gates count, 2 clock latency. Chabi et al. [c] proposed another structure of 29 cells, 4 gate counts and 0.75 clock latency. G. Singh et al.[d] presented one structure to realize XOR gate comprising of 28 cells, 3 gate count and 0.75 clock latency. A. N. Bahar et al. [e] have reduced drastically to 12 numbers of cell and 0.5 clock latency to design XOR gate. Later on R. Laajimi with A.N. Bahar have designed XOR gate consisting of 10 cells and 0.25 clock latency. In our work we have proposed an improved structure of 3 input XOR gate consisting of only 5 cells which indicate 50% reduction in no of cells, also in space reduction.

2. QCA background

The fundamental component of QCA design is quantum cell which is comprised of four quantum dots and two mobile electrons. Electrons can tunnel between dots quantum mechanically. The electrons can interchange their position between adjacent dots but cannot between cells. They are bound to take diagonal positions for columbic repulsion and two stable polarizations. Quantum cells are categorized as polarized and non polarized as shown in fig.1(a). One polarization, P (+1) is denoted as logic "1"and another one P (-1) as logic "0" as shown in fig. 1(b). The array of QCA cells form a binary wire through which data move due to columbic interaction as shown in fig. 1(c). Wires are realizable by connecting cells in series using two angular positions of cells 90^o or 45^o rotation. Operation of NOT gate is realizable by making two cells of opposite polarity (+1 and -1) as shown in fig.1(d). 3 input Majority Voter (MV) gate can be constructed using five numbers of cells as shown in fig.1(e). Operation of AND, OR gate is realizable making one input of MV to either P=-1 or P=+1 respectively. Majority gate is represented by the following logic function

MV (A, B, C) = AB + AC + BC

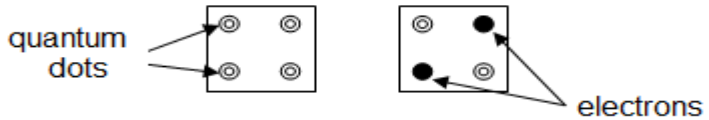


Fig-1(a) : quantum cells (non-polarized & polarized)

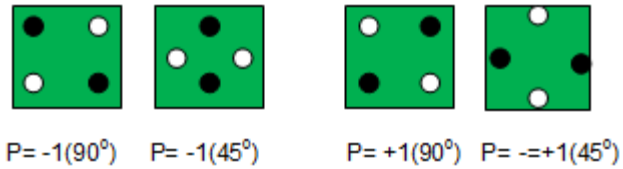
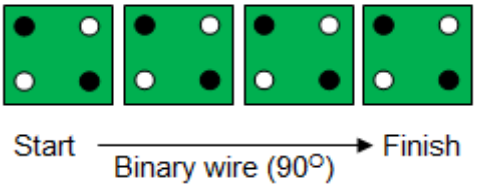


Fig-1(b) : cell polarization



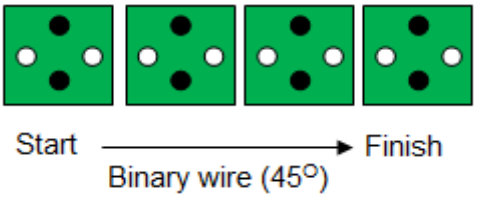


Fig-1(c) : Binary wires

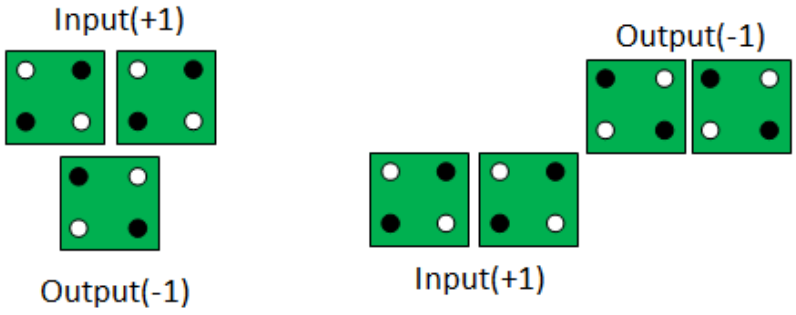


Fig-1(d) : NOT gate

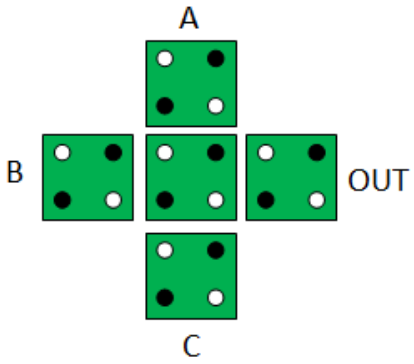


Fig-1(e) : Majority voter

For the proper operation of cells and to control the travelling of data through QCA circuits, clock is necessary. Unlike the use of clock in digital circuit, the quasi-adiabatic switching mechanism applied in QCA circuits. The clock cycle here has four phases, named as switch, hold, release and relaxes as shown in fig 2. In switch phase (t=0 to t=π/2) QCA cells initially are at non polarized and with low potential barrier. This potential barrier increased to high at switching. Next in hold phase (t=π/2 to t=π) barrier remains high. In release phase (t=π to t=3π/2) barrier changes to low and the cells become non polarized. Finally in the relax phase (t=3π/2 to t=π) cells maintain their low potential barrier.

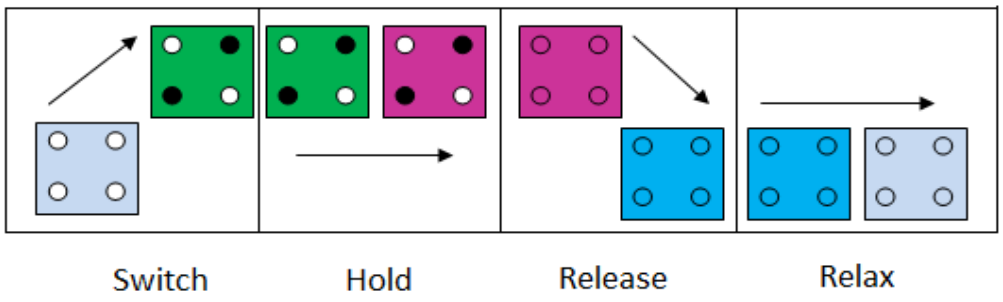


Fig-2 : Clocking in QCA

3. RELATED WORKS: - One of the most important logic gates is Exclusive-OR (XOR) gate. This gate has wide application in different digital logic circuits such as adder, subtractor, arithmetic and logical unit, error detection and correction circuits, reversible circuits, code converter and so on. As a matter designing of an efficient and high speed low power consuming XOR gate is one of the most important research areas in QCA. Different authors [12-17] had been introduced conventional XOR gate with low complexity. In older days designers used 2 input XOR gates to implement those useful circuits. A preview of previously designed 2 input XOR gates by QCA has shown in Fig. 4. But nowadays 3-input Exclusive OR gates are becoming useful for designing the maximum logic circuits. Till now, number of 3-input XOR gates have been introduced by several researchers. At the beginning Angizi et al. in [8], described an XOR gate of 94 cells and 0.073 μm2 area. Furthermore this gate has the time delay of 1.5 clock cycles. Ahmad et al. in [7] proposed a more reduced structure of 3-input XOR gate which is comprised of 14 cells, occupying area of 0.022 μm2 and output has delay of 0.5 clock

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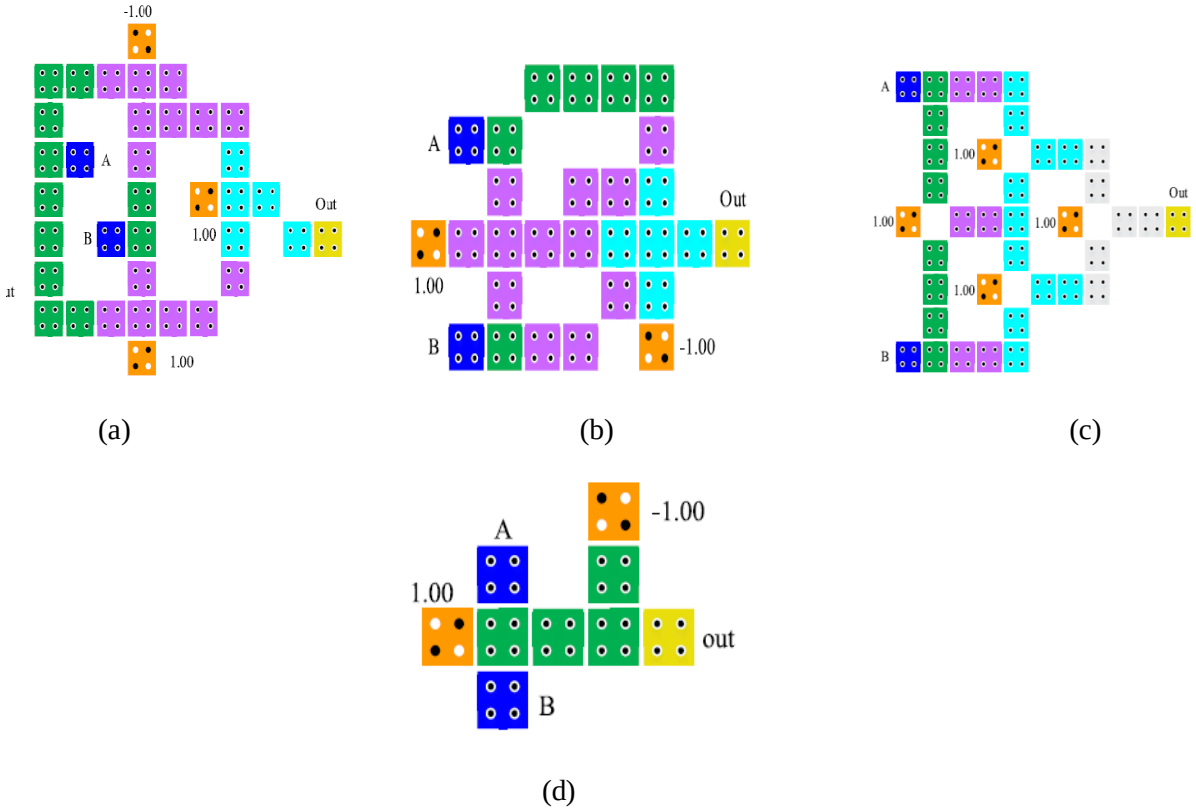
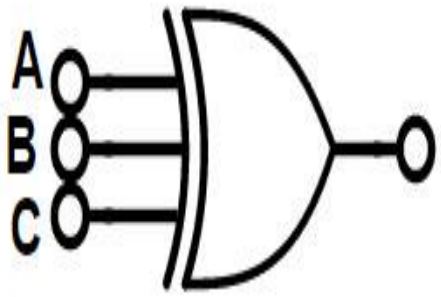


(a) (b) (c)

(d)

Fig-4: Various layouts of 2 input XOR gates designed previously in literatures [11]



Input A	Input B	Input C	Output Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Fig-3: Symbol of three input XOR gate and its truth table[21]

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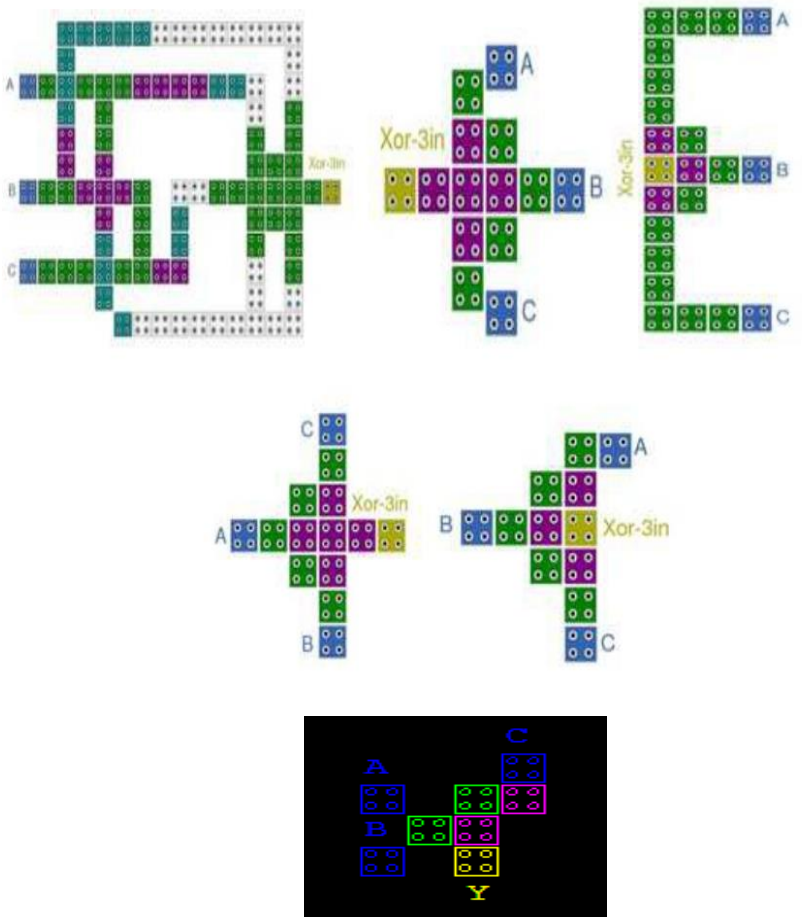

Fig-5: Depicts various layouts of previously designed 3-input XOR gate in QCA in literatures [20].

cycles. However, the said gate could not fulfil the expected optimization for the larger circuit. Bahar et al. have described with a compact XOR gate, in [18] that used 12 cells and occupied 0.012 μm2 areas. However, this gate is not suitable for designing large scale circuits. Another 14 cells XOR gate was proposed by Balali et al., in [19]. But this gate became physically impractical due to the use of half-cell transfer inverter gates. More recently, Gassoumi et al. in [20], designed a 3 input XOR gate which consists of only 8 cells with occupied area is 0.006 μm2 and uses only two clock phases to obtain the correct output. But this gate also could not achieve the expected optimization for the bigger circuits. Our proposed design of 3-input XOR gate is capable of achieving bigger designing optimization in more complex design platforms. The QCA layout of this gate is simple, appropriate and efficient for all logical functions compared to previous designs. Fig. 6(a) and 6(b) are showing the QCA layout of 3-input XOR gate and its simulation results respectively proposed by us, which consists of 11 cells with occupied area is 0.003 μm2 and completes in two clock phases to generate the correct output. The most important matter of this design is that it is implemented in single layer without any wire crossing and required only 11 cells, as shown in Fig. 6(a).

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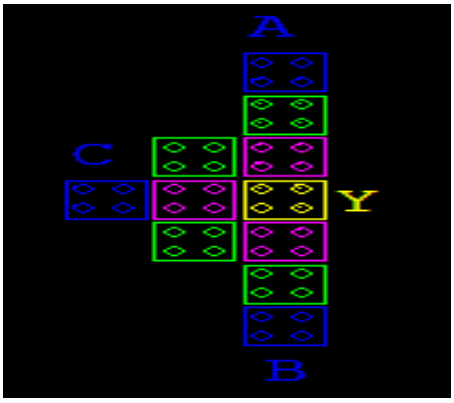

Fig-6(a): Layout of proposed 3 input XOR gate

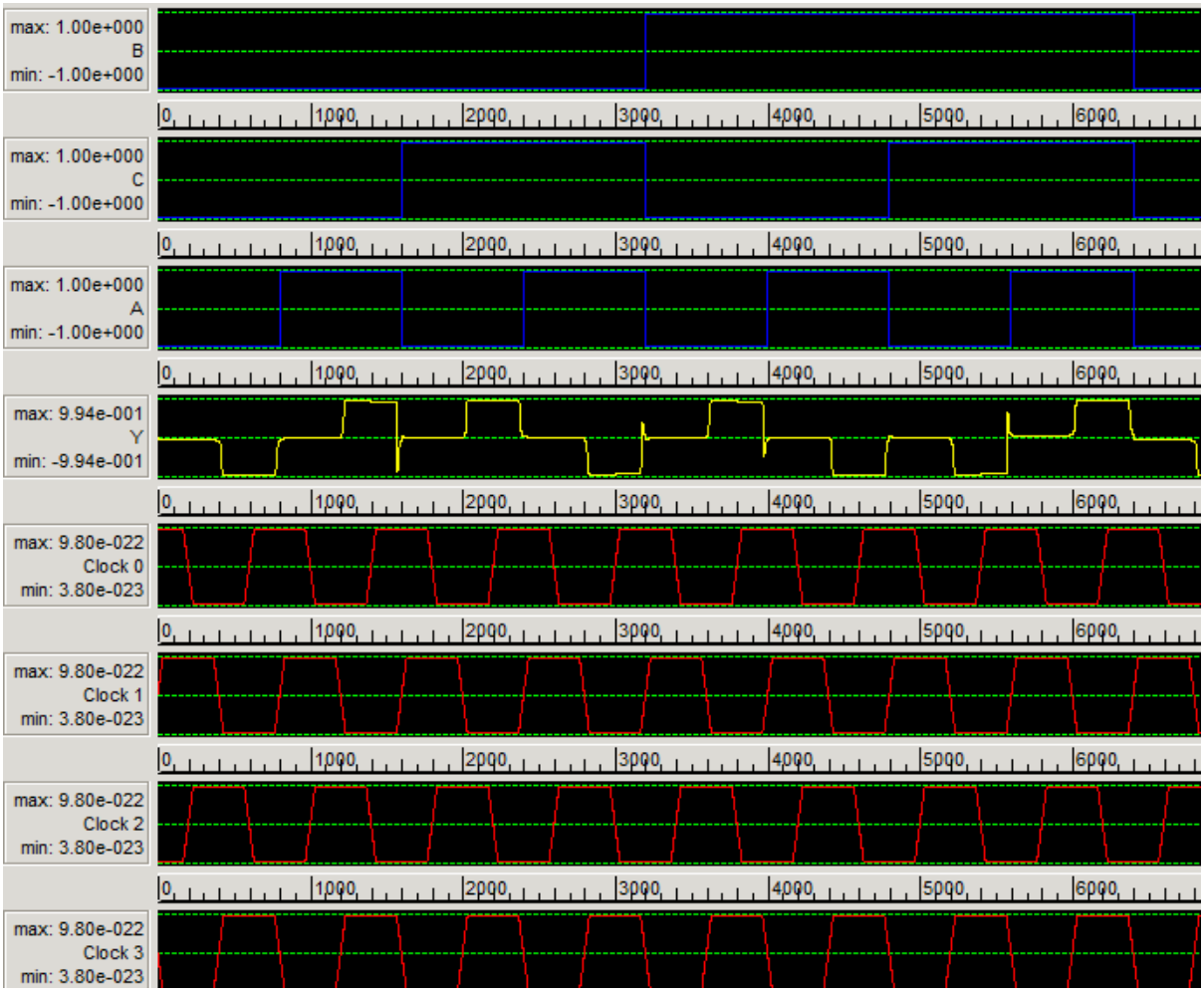

Fig-6(a): Simulation result of proposed 3 input XOR gate

4. RESULTS AND DISCUSSIONS

We have used QCA Designer (Ver. 2.0.3) tool to design and simulate the proposed QCA gate. The designer is set to a "bistable approximation" type (by default parameters) for working of simulation

engine and corresponding QCA parameters are presented in Table 1. Reduction in the XOR gate size will result in a subsequent reduction of the scaled-up circuits. The analogical results of the cell count, the consumed area and the latency of earlier works (3-input XOR) proposed by different researchers in references [7, 10, 8, 18] gate are shown In Table 2. Our proposed QCA XOR gate has achieved an improvement 8.33% in cell consumption comparison to the previous best design in reference [18].

Parameter	Value
Number of samples	12800
Convergence tolerance	0.001000
Radius of effect	65,000000(nm)
Relative permittivity	12,900000
Clock high	9,800000e-022
Clock low	3,800000e-023
Clock shift	0,000000e+000
Clock amplitude factor	2,000000
Layer separation	11,500000
Maximum iterations per sample	100

TABLE -1: Bistable approximation parameters model

Three-input XOR	Area(μm2)	Cell count	Latency
Ref [11]	0.073	94	1.5
Ref [7]	0.017	22	1
Ref [10]	0.022	14	0.5
Ref [8]	0.011	14	0.5
Ref [18]	0.012	12	1
Ref [20]	0.006	8	0.5
Proposed Design	0.003	11	0.5

TABLE 2 The comparison of the 3-input QCA XOR gates

5. CONCLUSIONS

Drawbacks of the conventional digital logic circuits are being improved by continuous optimisation of circuits using QCA. With this XOR gate plays an important role in digital integrated circuits and communication circuits. Parameters like reduction in area, less power consumption, improvement in speed etc. are demanding field of electronics engineering and computer science. Here we proposed a new three-input XOR gate in QCA regime consisting of 11 cells with an occupied space of 0.003 μm2. Hence, its performance figures are superior to the existing XOR structures in literatures in terms of area and cost. Most importantly, its input and output pins are full accessible as it is of scalable structure. Simulation results are showing that the proposed gate is one of the suitable techniques to develop efficient logic circuits for QCA following the specified protocol.

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