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Optimal GSDG MOSFET Design with Nature-Inspired Heuristics

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ABSTRACT

In this work, the small signal parameters of GSDG (Gate Stack Double Gate) MOSFET are optimized to design the deep submicron analog circuits. Two nature-inspired heuristics, DE (Differential Evolution) and HS (Harmony Search) algorithms are taken for this work. In the analog domain, the small signal parameters like the OFF-state current, trans-conductance and other design parameters of GSDG MOSFET are optimized in the regions of saturation and sub-threshold to achieve better electrical performances of the MOSFET. DE and HS based design results are much improved as compared to the previous literature.

Keywords *- GSDG MOSFET, Trans-conductance, OFF-state current, DE, HS, Optimization.*

I. INTRODUCTION

The Double-Gate (DG) MOSFETs has been used for the improvement of electrical performances in nanoscale digital and analog CMOS applications [1]. Wu *et al.* [2] proposed the leakage current control method by varying the shape of the gate of the device. Singha *et al.* [3] suggested that the improved delay provides better immunity to leakage current. Bentrcia *et al.* [4] also suggested a swing factor for the estimation of the device sub-threshold performance which varies with the gradual variation of the gate work function. Kaharudin *et al.* [5] have suggested that the Taguchi method can be utilized to obtain the optimal process parameters for the lower I_{OFF} value of the device. Medisetty *et al.* [6] have shown that the bias in compound back gate material helps in reducing short channel effects (SCEs). Nalawade *et al.* [7] discussed the propagation delay and dynamic power dissipation to overcome the problem of SCEs for the inverter circuit.

In this paper, the design of GSDG MOSFET [8-9] is investigated by utilizing DE [10-12] and HS algorithm [13-14] individually.

This paper is structured as follows: Section II describes the different small signal parameters of GSDG MOSFET and the detailed analysis of the Cost Function (CF) considered for the work. Section III describes the algorithms, i.e., HS and DE. Section IV presents the comprehensive simulation results, and Section V concludes the paper.

II. SMALL SIGNAL PARAMETERS FOR GSDG MOSFET

Under the gradual channel approximation (GCA) of symmetrical GSDG MOSFET, the drain current (I_{ds}) is represented as (1) [15].

$$I_{ds} = \mu_{eff} C_{oxeff} \frac{W}{L}\left[(V_g - V_0)^2 - \frac{8rk^2T^2}{q^2} e^{\frac{q(V_g - V_0 - V_{ds})}{kT}}\right] \quad (1)$$

where C_{oxeff} represents the effective capacitance oxide; L is the width of channel; W is the channel width; μ_{eff} represents the effective mobility; V_g is gate voltage; V_{ds} is drain to source voltage, $r = \left(\frac{\varepsilon_{si} t_{oxeff}}{\varepsilon_{ox} t_{si}}\right)$ is a structural parameter; $t_{oxeff} = \left[t_1 + \left(\frac{\varepsilon_1}{\varepsilon_2}\right) t_2\right]$ is the effective thickness oxide; t_1 is the thickness of the SiO_2 $(\varepsilon_{ox} = \varepsilon_1)$; t_2 is the thickness of the high-k layer; ε_2 is the permittivity of the high-k layer; ε_{si} is the permittivity of silicon, and t_{si} is the silicon thickness.

V_0 represents the work function of silicon thickness and is given by

$$V_o = \left(\frac{2kT}{q}\right) \ln\left[\frac{2}{t_{si}} \sqrt{\frac{2\varepsilon_{si} kT}{q^2 n_i}}\right]$$

The drain current (I_{ds}) in the sub-threshold region is represented as (2).

$$I_{ds} = \mu_{eff} \frac{W}{L} kTn_i t_{si} e^{\frac{q(V_g)}{kT}} \left(1 - e^{\frac{-qV_{ds}}{kT}}\right) \quad (2)$$

The trans-conductance is computed using (3).

$$g_m = \left.\frac{\partial I_{ds}}{\partial V_g}\right|_{V_{ds}} \quad (3)$$

The trans-conductance in saturation is derived from (3) and is represented as (4).

$$g_m = \mu_{eff} C_{oxeff} \frac{W}{L}\left[2 \times (V_g - V_0) - \frac{8rkT}{q} e^{\frac{q(V_g - V_0 - V_{ds})}{kT}}\right] \quad (4)$$

In the sub-threshold region, the OFF-state current is estimated by using (5)

$$I_{OFF} = I_{ds}\big|_{V_{gs}=0} = \mu_{eff} \frac{W}{L} kTn_i t_{si} \left(1 - e^{\frac{-qV_{ds}}{kT}}\right) \quad (5)$$

As g_m (4) acts as an objective function which is to be maximized. The OFF-state current, given in (5) acts as another objective function which is to be minimized. The overall cost function is obtained by 'weighted sum approach method' as presented in (6).

$$CF = w_1 \left(\frac{1}{g_m}\right) + w_2 I_{OFF} \quad (6)$$

As (4) has to be maximized, the reciprocal of it is taken in the overall cost function. w_1 and w_2 are weight functions. The device trans-conductance and the OFF-state current are equally important to the device designer to get the low power dissipation, high speed and high derived current. So, the weights 0.5 are utilized for each function. If

the application requires then the weights of this parameter can be varied for certain limit or some particular application. In this method, it should be guaranteed that the sum of all the weights is 1. Here, $w_1 + w_2 = 1$. Two objective functions are taken for this study, i.e., OFF-state current and trans-conductance as shown in (6). Row vector of the population matrix is represented by $X = (t_{si}, t_1, t_2, \varepsilon_2, L, V_{ds}, V_g)$.

The subthreshold swing (S) [1] is represented by (7)

$$S = S_0[1 + \Delta S]^{-1} \quad (7)$$

where S_0=60mV/dec represents the ideal value of the subthreshold swing and ΔS is the subthreshold swing degradation coefficient.

The sub-threshold swing (S) was extracted from the inverse slope of log I_{ds} vs.V_{gs} characteristic [16] and is given in (8).

$$S = \frac{\partial V_{gs}}{\partial \log I_{ds}} \quad (8)$$

III. OPTIMIZATION ALGORITHMS EMPLOYED

The DE algorithm was proposed by Storn and Price in 1995[10]. A meta-heuristic technique, mimicking the improvisation process of music players, has been proposed and named Harmony Search (HS) [13]. The description of DE and HS can be found in [10-14]. Different parameters used for DE and HS techniques are presented in Table 1.

IV. SIMULATION RESULTS AND DISCUSSIONS

In this paper, small signal electrical parameters of GSDG MOSFET are optimized by applying geometrical synthesis. The cost function for the design is individually optimized by utilizing HS and DE techniques implemented in MATLAB. The optimal dimensions (t_{si}, t_1, t_2, L) and electrical parameters $(\varepsilon_2, V_{ds}, V_g)$ are achieved from the HS andDE techniques individually. For the authentication purpose, TCAD is used to design the structure of GSDG MOSFET for electrical simulations. Table II shows the optimal GSDG MOSFET parameters. TCAD simulation results achieved from HS and DE-based optimal design of GSDG MOSFET are presented in Figs. 2-4, respectively. HS based design results in t_{si}=55nm; t_1=1.5nm; t_2=1nm; L=160nm; ε_2 = 25;V_{ds}=4.4V; V_g=4.9V;I_{OFF}=3.41X10^{-09}*A/μm;*g_m=5.14X10^{-2} *S/μm;* *S*=70.70 mv/dec; ΔS = 0.1513; *CF*=9.7276. DE-based design results in t_{si}=50nm; t_1=1nm; t_2=0.5nm; L=145nm; ε_2 = 25;V_{ds}=4.55V; V_g=4.95V;I_{OFF}=3.04X10^{-09}*A/μm*;g_m=8.32X10^{-2}*S/μm*;*S*= 68.76 mv/dec; ΔS = 0.1274; *CF=6.0096*. Fig. 5 shows the convergence plots for HS and DE-based designs of GSDG MOSFET. Both HS and DE yield better-optimised results compared to MOGA [8-9] in terms of device dimensions and electrical parameters as shown in Table II.

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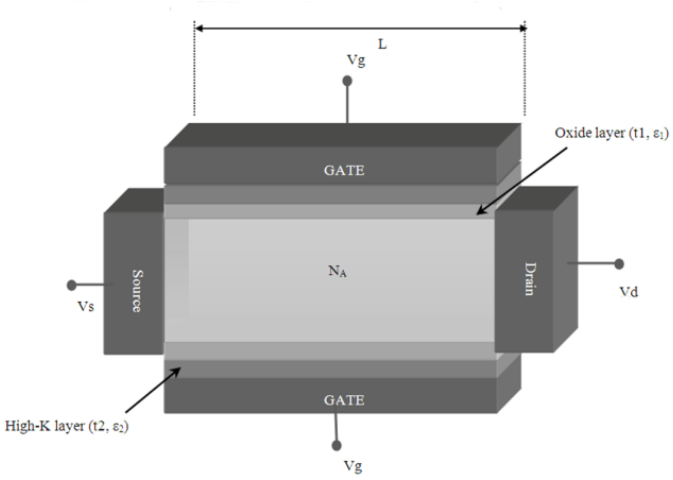

Fig.1. A cross-sectional view of the GSGD MOSFET device.

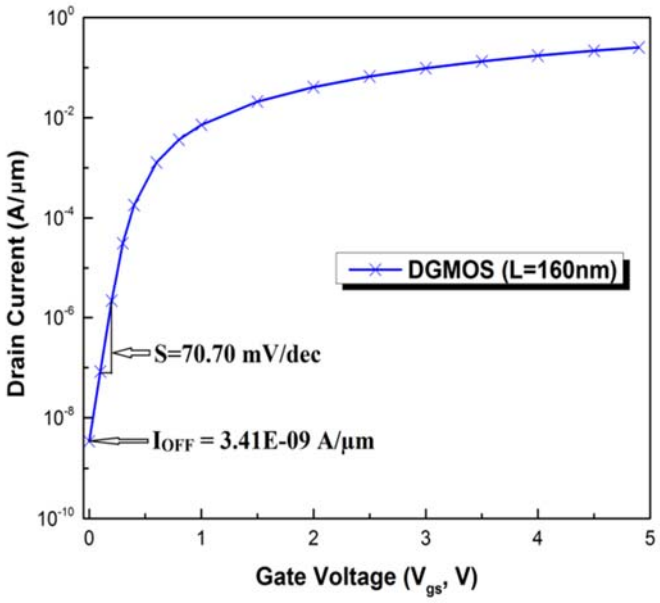

Fig.2. Drain current in OFF state for HS based design.

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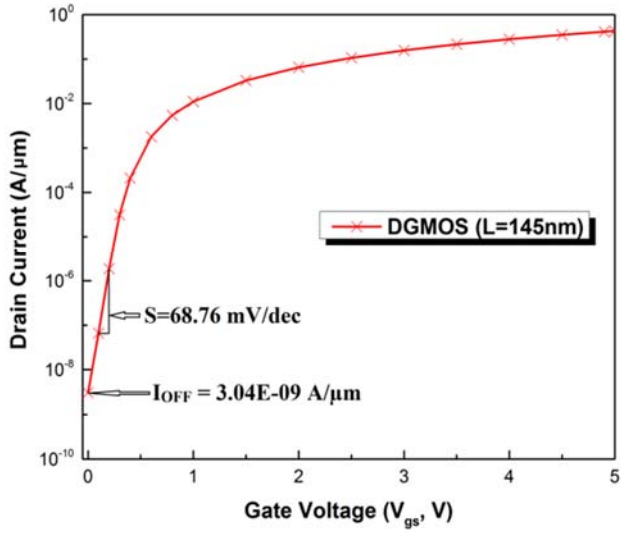

Fig.3. Drain current in OFF state for DE-based design.

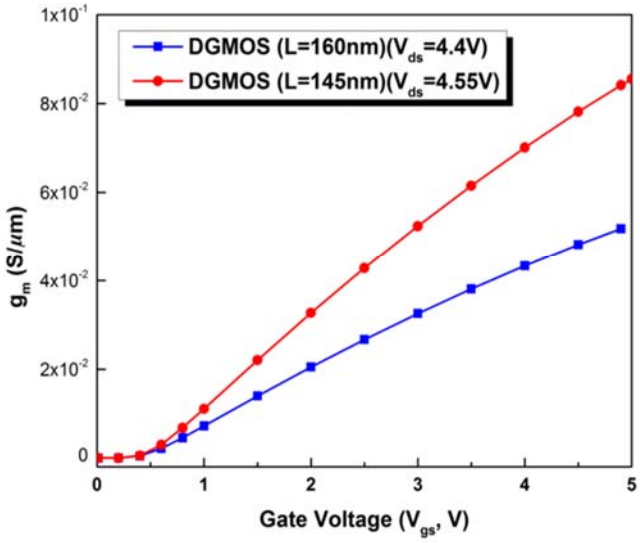

Fig.4. The plot of transconductance for different structures.

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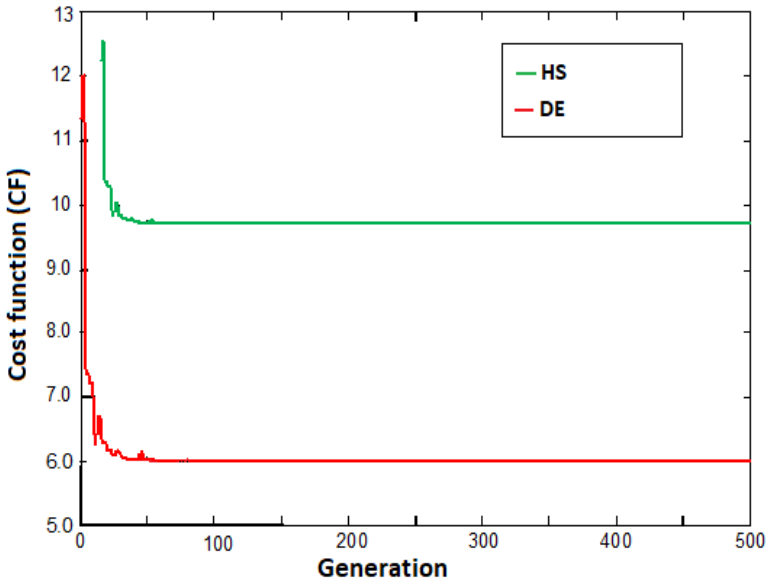

Fig.5. The plot of convergence profile for DE and HS algorithm.

TABLE I. Different Parameters for DE and HS

Parameters	**DE**	**HS**
Population Size	10	10
The dimension of the optimization problem (D)	7	7
Iteration Cycle	500	500
HMCR	-	0.6
PAR	-	0.3
BW	-	0.01
NI	-	20
F	0.5	
C_r	0.8	

TABLE II. OPTIMAL GSDG MOSFET PARAMETERS

Symbol	Quantity	MOGA [8-9]	HS	DE
t_{si} (nm)	Silicon thickness	49.999	55	50
L (nm)	Channel length	144.7187	160	145
V_g (V)	Gate voltage	4.9999	4.9	4.95
V_{ds}(V)	Drain source voltage	4.8512	4.4	4.55
t1 (nm)	Thickness of the SiO2	0.5046	1.5	1
t2 (nm)	Thickness of the high-k layer	0.5010	1	0.5
V_0 (V)	Threshold voltage	-	0.3858	0.3907
$\varepsilon 2$	Permittivity of the high-k layer	39.9999	25	25
I_{OFF} *(A/µm)*	OFF-state current	$9.0044X\ 10^{-14}$	$3.41X10^{-09}$	$3.04X\ 10^{-09}$
g_m *(S/µm)*	Transconductance	$1.7374\ X10^{-2}$	$5.14X\ 10^{-2}$	$8.32X\ 10^{-2}$
CF	Cost Function	28.877	9.7276	6.0096
t (s)	Execution time	20	17	12
S (mv/dec)	Subthreshold swing	-	70.70	68.76
ΔS	Subthreshold swing degradation coefficient	-	0.1513	0.1274

V. CONCLUSION

In this article, small signal electrical performance parameters of GSDG MOSFET are optimized by utilizing HS and DE techniques in sub-threshold and saturation regions for deep submicron CMOS applications. Both HS and DE have efficiently discovered the optimal dimensions of the GSDG MOSFET and improved small-signal electrical performance parameters with respect to the previous literatures.DE shows to be a better optimizer for the device considered in this work.

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