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ANALYSIS OF DFT AND BIST ARCHITECTURE FOR ENHANCED SECURE TESTING OF VLSI CIRCUITS

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ABSTRACT: An efficient Design for Testability (DFT) has been a significant concern for the present VLSI engineers. An ineffectively designed DFT would result in losses for manufacturers with a considerable rework for the designers. BIST (Built-in Self-Test) is one of the promising DFT techniques is quickly changing with the advances in innovation as device contracts. Due to the developing complexities of the equipment, the pattern has shifted to remember BISTs for superior hardware for disconnected just as web-based testing. Work done here includes testing a 'Circuit Under Test' (CUT) with a built accordingly analyzer and vector generator with a monitor to control all the exercises. The utilization of low progress vector generator here 'Bit Swapping Complete Feedback Shift Register' power has been decreased impressively when contrasted with traditional 'Linear Feedback Shift Register' techniques. This study depends on DFT and BIST testing of VLSI and Design-for-testability techniques that will permit DFT experts, and VLSI designers to master rapidly System-on-Chip Test architectures, for test troubleshoot and finding of digital, memory, and simple/blended signal designs.
Keyword: BIST, DFT**,** CUT, Virtex.

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I. INTRODUCTION

During the most recent couple of years, the development of the test has carried it closer to design, in this way spanning the conventional hole among designs and testing. Test requirements, once observed as a bit of hindsight after design, are presently corresponding to the design movement. The job of testing is to guarantee that lone the imperfection free ICs advance toward the shoppers. Headway in the creation and hardware innovation makes it conceivable to incorporate a large number of transistors on a small bit of silicon known as Integrated Circuits (ICs). These ICs can perform a huge number of capacities in the ideal succession. The three key building disciplines associated with the assembling of these ICs are Design, Fabrication, and Test. The pattern towards an expansion in design multifaceted nature and speed of activity combined with the requirements for development in the building forms for decreasing item cost is driving enhancements in all parts of device design, manufacture, and test.

Power dissemination is a significant design concern and has become a key test as it concerns an enormous range of items extending from superior figuring to remote correspondence. So as to meet low energy requirements, some new low power techniques that incorporate circuits, architectures, and algorithms have developed. The tight limitations on the power dissemination of VLSI circuits have made new difficulties for testing low power VLSI circuits which need to beat the conventional testing techniques that don't represent power dispersal during the test.

The greater part of the current low power techniques are planned for lessening the exchanging action during the practical activity that may strife with the test flow. For instance, a mind boggling IC may devour three to multiple times more power during testing when contrasted with its useful activity. Henceforth, power management isn't simply bound to the design space just yet is a significant test during testing also. The examination efforts in the work announced here is focused towards low power testing of VLSI modules that is a sub-issue of the general objective of VLSI testing.

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II. DESIGNS FOR TESTABILITY (DFT) AND BIST

DFT techniques are those design techniques that make test age and test application financially effective. As it were, they are the design strategies that encourage increasingly careful and less expensive testing. DFT is accomplished by including additional test circuits and this test circuit gives improved access to the inside circuit hubs. It assumes a significant job in the advancement of test projects and goes about as an interface to test application and conclusion. DFT is principally characterized into two sorts: Ad-hoc and Structured DFT techniques. The specially appointed technique depends on great design understanding to discover and fix the issues. It isn't utilized for testing huge circuits since it is a serious strategy and doesn't ensure great outcomes from ATPG. In Structured DFT techniques, additional rationale and signals are added to the circuit to allow the test as indicated by some predefined methodology. Regularly utilized organized strategies incorporate sweep, incomplete output, BIST, and limit filter. In the output design, flip-flops are supplanted by the sweep flip-tumbles and associated with form at least one shift registers in the test-mode.

Design for Testing (DFT) and Built-in Self-Test (BIST) are the strategies to test the chip at the design stages for 100 percent stuck to blame. DFT has a few techniques to expand controllability and discernibleness, for example, check design strategy, on-chip equipment for test design age, and information pressure strategies. Different strategies for DFT are joined to form the BIST conspire. The significant BIST plans are joined test design age, built-in assessment, self-test, apportioning, multiplexer test point inclusion, sequential output, and irregular test design.

There is various devices accessible to distinguish the imperfection in the chip at the design level itself. Design check systems and PC supported design methods are utilized to recognize the deficiency in the chip during the design stage itself (Tory Nagle et al. 1989). In the event that there is any assembling shortcoming, that can be recognized by the creation test. Physical imperfections can typically occur in the chip which will prompt breakdown of the chip from the ordinary expected capacity. The deformities regularly happen are mass silicon absconds, substrate mounting surrenders, substrate surface deficiency, holding abandons, molecule tainting, warm crisscross electrical dependability, oxide imperfections, and metallization deserts (Tory Nagle et al. 1989). The stuck to blame model portrays the physical imperfections for stuck at '0' and stuck at '1'. The stuck to blame model itself adequate to recognize an assortment of flaws referenced previously. The stuck to blame model is utilized to produce test designs.

BIST is a design strategy of testing the circuit under test by putting the testing capacities inside the CUT itself. The three significant structures of BIST is a tested example generator, yield analyzer, and test controller. The capacity of the test design generator is to create the necessary test design for the circuit under test. A portion of the instances of test design generators are Linear Feedback Shift Register (LFSR), counter or ROM with as of now put away testing information. Reaction analyzer is a sort of Comparator, which stores model yields for correlation with present yields of the circuit under test. The rest controller is circuit to provide order signal to the test design generator to discharge test designs for testing. It additionally impart signs for the reaction analyser to break down the current yield with the as of now put away yield. The test related capacities are completed in the test controller.

III. PROPOSED METHODOLOGY

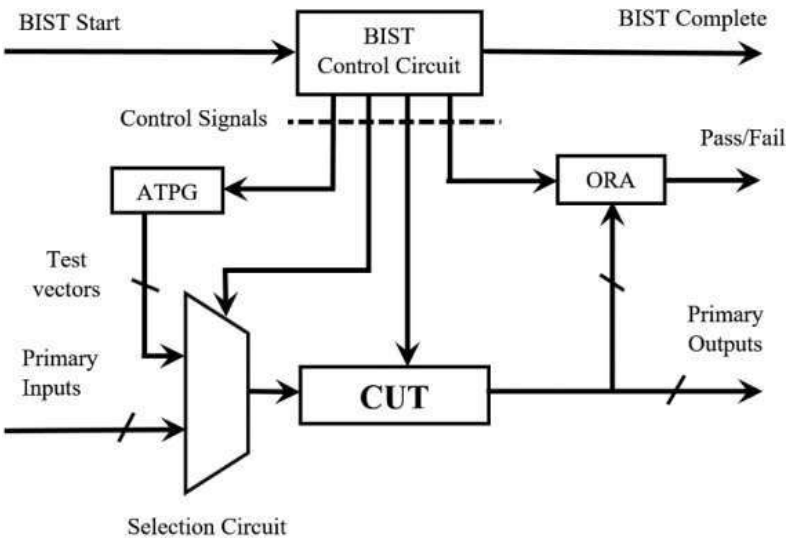

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Figure 1: BIST Block Diagram

Built-In Self-Test (BIST) is a DFT philosophy that tests the pointed circuit by checking for shortcomings and produce a reaction saying it has finished the assessment or not [8]. This self-test highlight accompanies a tradeoff – More zone requirement and higher power utilization because of additional circuits added to the useful circuit. Automatic Test Vector Generator (ATPG) and Output Response Analyzer (ORA) are the most basic piece of this extra circuit. The most generally acknowledged vector generator is a linear feedback shift register (LFSR) which yields pseudorandom test vectors. Alterations are performed on the old-style model to improve any of the previously mentioned issues. One of them is utilized in the proposed BIST execution. Counters, pressure-based, collectors, signature investigation, focus, and so forth are some of ORAs which decreases the yield reaction and makes it simpler for the controller to give results [8]. The alleged brilliant vectors (shortcoming free reactions) are put away in ROM memory of the circuit. Figure 1 shows essential squares fabricating a BIST.

The proposed scheme for testing is designed dependent on three elements: 1) FPGA test time, 2) decreasing conditions on TPG-CUT entomb associates, and 3) the simplicity of following the shortcoming area in the device. This area dissects the BIST strategies for testing FPGAs that have been proposed previously and afterward looks at it to the proposed plot. BIST architecture can be mapped on FPGAs in various manners. The least difficult way is the place each TPG-CUT-ORA involves one configurable rationale square (CLB). This strategy, albeit basic, is very tedious.

The strategy laid out in [9] utilizes Circular BIST examination based ORAs to look at the yields of numerous indistinguishable CUTs. In spite of the fact that it builds the exactness of deficiency location, it expands the heap on TPGs as this strategy utilizes two TPGs for the whole column. Thus, the precision of cell choice is subject to interconnect. Along these lines, following a mistake to a certifiable flaw or a defective TPG is very troublesome in this technique. The re- programmability of FPGAs is all around abused in [10]. Be that as it may, outside memory is required to store the BIST setups and the time required to download and execute the BIST is impressive. The BIST conspire proposed in [11], has TPG in an alternate CLB and the plan proposed in [12] has TPG/ORA in an alternate CLB, consequently to test all the cuts in a CLB utilizing [11] [12] would take four meetings. Additionally, these techniques are subject to TPG- CUT-ORA interconnects for sending the right location and discovery of defective yield. Besides, each CUT needs TPG and an ORA, and in these past investigations each TPG/ORA possesses a whole CLB. So in one meeting just 50% of the CLBs go about as CUTs. Thus, they had the option spread half CLBs in one test meeting. The present work proposes an alternate BIST architecture where the TPG, CUT, and ORA are fused into one CLB. A different TPG and ORA is utilized for each CUT. Numerous indistinguishably arranged TPGs gracefully test examples to indistinguishably designed CUTs.

A single CLB in a Virtex-4 FPGA has 4 cuts (Slice L and Slice M). Each cut has two LUTs. The TPG is built utilizing four LUTs. It produces delivers 0 to 15. For testing utilizing March algorithms, the addresses should be produced consecutively. A straightforward up/down counter is utilized for this reason. A solitary Slice L is utilized to fabricate an ORA and the CUT is developed utilizing a Slice M, since Slice M contain LUTs which can work as RAMs. Thus, utilizing the proposed architecture the LUT RAMs in a CLB can be tested in two test meetings.

Detection of the faulty LUT/RAM (F or G) is conceivable through the ORA output which have two broken signals, one for each LUT. On the off chance that all the ORA yields (F1-F4 or G1- G4) show "0000" at that point it tends to be inferred that no issue exists in the line. At the point when a flaw exists, the comparing signal goes high. For instance, when the ORA yield shows F2 "0010", at that point it tends to be resolved that the shortcoming exists at CLB#2 of F LUT. Also, "0100" (CLB#3) and "1000" (CLB#4) recognize the deficiency. The specific location at which the issue is available can be found from the TPG address.

IV. RESULT

The useful model of the Virtex-4 FPGA is executed utilizing Verilog and reproductions are done in ModelSim. The advanced March C-the algorithm is utilized for testing purposes. Beginning reenactments are managed without presenting deficiencies and afterward the reproductions are accomplished for every one of the individual shortcomings: stuck at, transient, IRF, RDF, DRDF, DRF, and a location decoder. The nitty gritty clarification for the read shortcomings is given below

Case I: Incorrect Read Fault at Address 1001

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IRF is presented at the location 1001 of GLUT in CLB#1. Because of this, the read activity that is performed on cell 9 consistently restores erroneous rationale esteem despite the fact that the right worth is still put away in the cell. The shortcoming is distinguished by the March component M1.

Case II: Read Destructive Fault at address 1010

RDF is presented at address 1010 of GLUT in CLB#1. Because of this, at whatever point a read activity is performed on cell 10, the information put away in the cell changes to its supplement and returns a mistaken an incentive at the yield. The shortcoming is distinguished first by March component M1. The distinction among RDF and IRF is that on account of RDF the substance of the cell changes. Notwithstanding, on account of IRF, the substance of the cell continues as before.

Case III: Deceptive Read Destructive Fault at address 1100

DRDF is presented at the location 1100 of FLUT in CLB#1. At whatever point cell 12 is perused for anticipated worth, it at first returns the real worth and afterward the following read it restores its supplement on the grounds that the primary read changes the substance of the cell. The issue is recognized by M4.

Case IV: Data Retention Fault at address 1011

DRF is presented at the location 1001 of FLUT in CLB#1. At whatever point cell 9 isn't gotten to for a specific timeframe and read for anticipated worth, the condition of the cell flips and returns an erroneous incentive at the yield. The cell is set in an inactive state utilizing the HOLD order in the March algorithm. The Fault is recognized by M4.

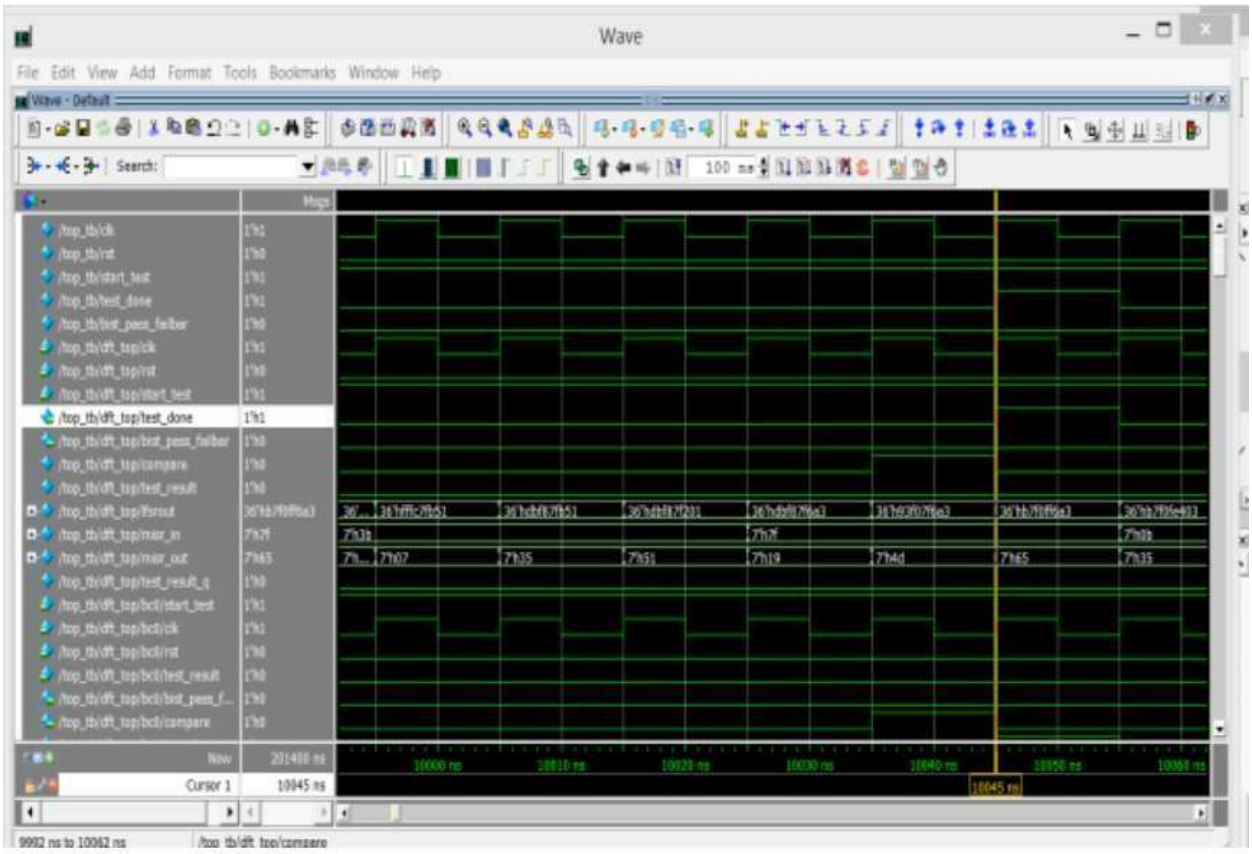

Figure 2: Simulation Result

Table 2: Fault Coverage and Test Time taken to Cover Faults

No	Fault Models with fault at address 0001	No. of clock Cycles taken by the proposed method	No. of clock Cycles [10]
1	SAFI	18	17
2	SAF0	34	77

3	ADF	34	77
4	Up-TF	34	77
5	Down-TF	76	83
6	IRF	18	NA
7	RDF	18	NA
8	DRF	108	NA
9	DRDF	109	NA

V. CONCLUSION

BIST is created and executed to test the memory assets of Virtex-4 FPGAs utilizing a streamlined March C-algorithm. The quantity of CLBs in a solitary meeting utilizing the proposed BIST plot is expanded by 54% and a half when contrasted with [9] and [11] [12] separately. The number of cuts involved by the BIST conspires, the number of lines of VHDL code for the usage of the BIST plot. Improved March C-algorithm requires 12n tasks to totally test the memory for the nearness of stuck-at, transient, IRF, RDF, DRDF, DRF, and address decoder issues. Accepting a clock time of 5 MHZ, the specific number of clock cycles to identify the flaw and the time taken to find the issue is determined, contrasted, and [11], and recorded in Table 1. Reproductions are finished utilizing ModelSim to confirm the fruitful testing and flaw area capacities of the methodology.

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