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DESIGN AND VERIFICATION OF DUAL LOGIC LASMAS STATE MACHINE FOR SOC

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ABSTRACT: The dual-core embedded System-on-Chip (SoC) will be used especially in high processing demands such as video processing, audio processing and sometimes mixing of both audio processing and video processing. On a single chip it can design two processor cores and different interfaces to restrict a bus known as 128-bit ARM advanced microcontroller bus architecture AMBA. The Lasmas state machine output can able to determine the time of latch level produced by the register. The coordination of the bus and to implementation some responsive functions will be developed by the RISC (reduced-instruction-set computing) core. The development of transformational tasks with better accuracy and regular behavior can be implemented by DSP (digital signal processing) core. The DSP design can be enhanced to a great extent by executing all these tasks. The Transport Triggered Architecture (TTA) is used to design a DSP core which can minimize the hardware complexity, increase the flexibility and reduce the market time to a greater extent. This system will be expected to give optimum performance at suitable operating frequency. Finally it will consume very less amount of power. The design and implementation of dual logic Lasmas state machine for SoC will be implemented using TTA-DSP architecture.

KEY WORDS: Embedded system, Lasmas, TTA, DSP, system-on-chip, RISC, Processor core.

I. INTRODUCTION

An embedded multimedia system computing tasks will be generally divided into control-oriented and data-dominated tasks. In general these two methods of computing platforms can be used for media processing. It is required to process both control functions and data functions. The advanced reduced instruction set computer (RISC) designs will be enhanced for a better data-concentrative functions by comprise accumulators, single instruction multiple data (SIMD) data paths, or particular devices to have the capability to implement data-concentrative functions [1]. However, the execution not that much good when compared to digital signals processing (DSP) with similar computing resources. Since data- concentrative functions will be much clear from normal calculation. The green public procurement (GPP) specifications will be available in DSP but these specifications are not perfect [2].

The primary responsibility of the design engineer is to fabricate a millions of transistors on a single chip to meet requirements of fast developing fields like mobile communication and digital signal processing (DSP) [3]. This technology is called as integrated circuit (IC) and this will lead to diminishes power consumption, delay and area. In present days there is a remarkable growth in the engineering and technology fields like industrial, mechanical, electrical and electronics. The integration density increased to double for every two years as described by the Moore's law. Due to this growth, at a fixed area of chip the complexity of IC will be enhanced drastically [4]. The design engineers will be developed a new technologies in order to manage the complexity with large chips. There is lot of limitations in WISHBONE open core technique especially in terms of system design. In this paper all these problems will be solved by using dual logic LASMAS state machine for SoC design.

II. LASMAS STATE MACHINE FOR SOC

An IC with a single chip and fabricate total circuit on a chip, is popularly known as a system on chip (SoC). The SoC means an entire system on a single chip. Based on the size of the chip that a system can able to reduce , it has various applications such as artificial intelligence, communications and signal processing .The major requirements of this design is minimize in power, low form factor and less total cost . The better performance can be achieved with a less occupied area by using a SoC technique. The pre designed and pre verified cores are key points in SoC design. The design reuse technique uses reusable IP (intellectual property) blocks to assist in the concept of integration. The concept of reuse technique can also capable to

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fabricate huge number of chips with a low power, high quality and low cost. For multimedia processing dual-core SoCs are most suitable architecture.

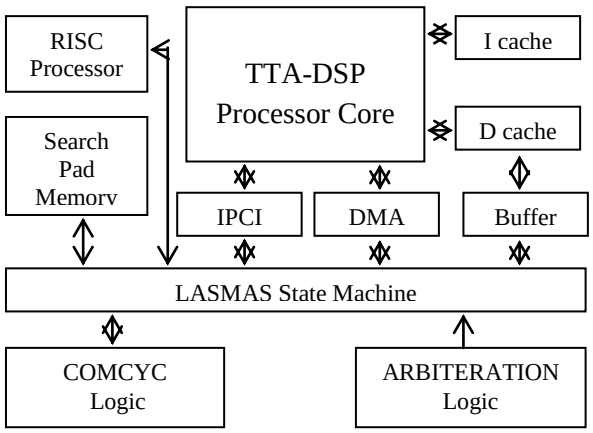

Fig. 1: Architecture OF Dual-Logic LASMAS State Machine for SoC

The SoCs can perform parallel functions depends on type of core used for design purpose. A different algorithm will be implemented by each core. All these algorithms can easily accessed by related core. Open multimedia applications platform (OMAP) is implemented by Texas Instruments, was a progression of picture/video processors. They are restrictive system on chips (SoCs) for compact and mobile multimedia applications. To increase the execution speed of an embedded processors there are various strategies. The parallel computing method is available in this SoC architecture and this type of computation provides simultaneous operations so that it reduces required time and cost. The parallel computing will be available in three levels such as data level, task level and instruction level. Sometimes it can perform all these functions at time also. For repeatedly occurring operations with large circuitry, it can assign specialized instructions to increase the speed of multimedia processor.

The SoC design methodology has several advantages and to meet all these benefits this technique can have various challenges such as area, design complexity and cost. The SoC design technique will also require a specialist designer who is perfect in hardware as well software. It's a very important aspect to implement a genuine test methodology for a test after manufacturing. The design time and cost of the design increased to meet perfection in integration of all these issues. The platform based SoC has proposed to handle integration difficulties and reduction in design time. It is very important to use a batter platform for design in terms of fabrication issues, cycle time. Any new design can be easily derived from available original platform. This platform should have an extraction level with different ideas to reach the particular product to a lower level. A new thought such as open core SoC design technique can able to provide all the needful information about the hardware. This core can able to implement lot of prior synthesized and verified hardware requirements under the some license of General Public License (GPL) and Lesser General Public License (LGPL).

The dual logic for Lasmas state machine will be depicted in fig 1.The SoC architecture contains two cores and these cores have built with various architectural plans to optimize a particular task. The RISC processor accommodating with the scheme for promotion of academic and research collaboration (SPARC V8) architecture and the processor have 32 bit data bus. Here two major tasks will be performed; they are processing of number of bits and commanding over a system. The TTA-DSP design is based on very long instruction word (VLIW) processor. This design is mainly used to compute the DSP processors with high throughput in filtering applications. The ease of programming and parallel computing at data level can achieved with help of the TTA-DSP core. This core is designed by using TTA architecture. The DMA (direct memory access) tunnels can capable to transfer the data directly DSP cache and external memory, without impacting the core. The most regularly used information usually known as constant data can be stored by using a 32 KB scratch pad memory. The process of retrieving the data from external memory will lead a more time consumption. The protection of memory access among D cache and system bus can be implemented by a buffer. The IPCI (Inter Processor Communication Interface) will be used to handle communication between two processors.

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In TTA –DSP processor architecture the DSP core has parallel computing capability and it is designed by using VLIW design. TTA (Transport Triggered Architecture) can be used to design a DSP processor core. In this architecture there is a possibility to get easy design issues, required functions and flexibility in programming so that this architecture will be well suitable in embedded DSP applications. The DMA functional unit which is inbuilt with architecture can used to transfers the prior fetching instruction and data, from I cache to D cache. Transport Triggered Architecture (TTA) operation can be depends on data transport. There is a lot of difference in the way the operations are executed both in advanced TTA and conventional architecture. In TTA the operations takes place as a function of data transports instead of triggering data transports. When the data is written to operand registers then the processing of task begins. From this design it is obvious that one data transport is required to be clearly placed in the instruction. In fundamental TTA architecture, the data path will be implemented by several function units (FU) and register files (RF). The interconnection network which comprise of required number of buses can be used to data transfers between the units. This design architecture is much workable since its components such as the number of FU, RF ports, buses and bus connections will be modified unrestrictedly. The processing time can be decreased by adding connections and buses so that more data transfers will be processed in parallel.It is very important to add some application specific operations at any time during the process for a optimum level performance of the design. The designer have a capability to add some operations based on demand of application into instruction set. This can make TTA architecture more reliable in the market. This architecture is so simple and flexible to design. The performance of this architecture becomes efficient because very complicate operations become insignificant. The various tools based on client for TTA can able to make a programmer to perform complicated algorithms into coding form. This coding form is simple and easy to understand. The mapping a code and generated parallel code will be handled by a scheduler. The simulator can function the verifying and implement the available codes.

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TTA-DSP Architecture will gives more reliability. Transport Triggered Architecture (TTA) is much useful for application specific processor design because of its features like flexibility and scalability. Based on the specifications of signal processing, the TTA-DSP design will be implemented. Various operations can be executed by using customization of different function units. Some special instructions will be added to instruction set. This architecture has various functional units to perform design process well. There is a functional unit which exclusively designed to implement trigonometric function calculation, called upper triangular portion of matrix (TriU unit). All these function units are applied to 8 buses, which can perform or execute 8 data transfers at a time. SIMD data path is implemented in the IFU to utilize a data level parallelism to a great extent. The rich integer functions can be in consolidated by IFU.

There are some data manage operations like mix, shuffle, pack and unpack can be implemented in addition to fundamental basic operations such as, add, sub, multiply, sub word. In the structure of IFU four IFU units are used to escape from hardware resources dispute. In this architecture one IFU processing multiply- accumulate operation and another IFU is implementing add operation of 8 bytes. Another function unit such as TriU, which will be designed based on coordinate rotation digital computer (CORDIC) algorithm. In this way this unit can compute several trigonometric functions just in 32 cycles, which is an optimized technique compare to other methods in which more time and place consuming will be takes place. Based on number of FU are fabricated on a single chip in VLIW machines the complexity of the register file increased quickly. In this situation the area of the centralized register files increases as N3, the delay as N3/2, and the power dissipation as N3 for N concurrent function units. The number of function unit increases then the register file will influence the delay, area and power dissipation. This problem can be resolved in TTA architecture by partitioning the register files. On demand four register files can be retrieve by any function units in TTA-DSP architecture, due to this the complexity of design will reduced without performance degradation. Data can be forwarded from one FU to another directly. Hence several middle results savings are bypassed. Here each FU has its own register. The increased FUs in a system will cause a register to dominate delay, area and power consumption. The separated registers in TTA can able to resolve this issue. Whenever it's needed, the TTA-DSP can select any FU. In this way the number of circuits requires to perform a particular function can reduced without any impact. Here every FU contain its own registers and the information can be moved directly from one FU to another. In this process so many middle results are formed.

The software development will be explained in this section. The hardware issues, code optimization, instructions allocations and VLIW parallelization will be developed with help of a technique called optimizing compiler is available in a TTA-DSP software design. By using this compiler, C programs will be comfortably mapped to the TTA-DSP hardware architecture, where as in some computation core algorithms this mapping is a much complex task. This optimized compiler will be enhanced to implement sub word data types for SIMD. The

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simulator can be used to improve design considerations and instruction set in a TTA-DSP cores. The same core can be utilized even for future application improvements.

The Inter-Processor Communication Interface will be depends on DSP processor. Many DSP kernel algorithms are available and these are proceeds on the DSP processor. By using RISC processor the absolute application will be executed. In this control oriented part can be processed first and DSP kernel algorithms will be taken if necessary. So while the application is in processing the inter-processor communication is always present. Through an interrupt technique the two techniques like the RISC processor and the DSP processor communicated. This advanced methodology generates straightforward software protocol between the two cores. The integrated personal computer interface (IPCI) design consists of 6 registers for better communication mechanism. Among these 6 registers, three registered from RISC to DSP, remaining three are from DSP to RISC. These two sets of three register are almost same. So the 3 registers are

- **Instruction register:** This register is used to transfer a instruction to the interrupted processor in the interrupting processor.
- **Data register:** This register is used to transfer a information to the interrupted processor in the interrupting processor.
- **Flag register:** This register will be cleared whenever the interrupt is responded interrupting processor. This register will be set if, writing to the instruction register an interrupt will be generated to the other processor.

The interrupt processor should permit the interrupt when it's completed the reading the data register and the instruction register. If the instruction is read by the interrupt processor then obviously the flag register get cleared and interrupt is reset. No interrupt will be produced and forward to the processor whenever the interrupt is masked in the interrupt handler. If the interrupt is unmasked then automatically the flag register will be set. In this scenario an interrupt will be occurred. The Arbitration Logic will be generally used in shared bus architecture. To permit the approach of the bus to a master, a device called arbiter (ARB) will be utilized in shared bus interconnection. It is a four levels and round- robin arbiter (RRA) as shown in fig 2. The round-robin arbiter gets the access a bus on rotation condition just like a rotary switch. In this rotary switch design, the arbiter gives a authority for a master0 on its demand. The arbiter will be turned to the next position and give permission to master1, immediately after master0 request was completed. The arbiter ignores a particular level and moved to the next level, whenever the master1 doesn't make a request for bus. So in this way in round-robin arbiter both masters get equal number of chances to get bus access. The RRA is much useful in the data acquisition systems, in which data are placed via shared memory. An arbiter contains arbitration logic, COMCYC logic, encoder logic, and LASMAS logic and register blocks. The COMCYC indicates weather the bus is free or busy and also it conveys that which master has been granted the bus. The bus requests came from four masters will be represented by the four inputs i.e. CYC0-CYC3. If master wish to get access of a shared bus it sends concern CYC signal then based on the accessibility of the bus the arbiter sends concern four grant lines i.e. GNT0-GNT3. The CYC0-CYC3provides the input COMCYC logic and produces a COMCYC signal will be produced. The master requests a bus and is accepted by the arbiter, if ICOMCYC is high. The encoder logic encodes the (GNT3-GNT0) to GNT (1...0). GNT (1..0) the instruction COMCYC for the purpose of aware that which master has been get permission to access bus.

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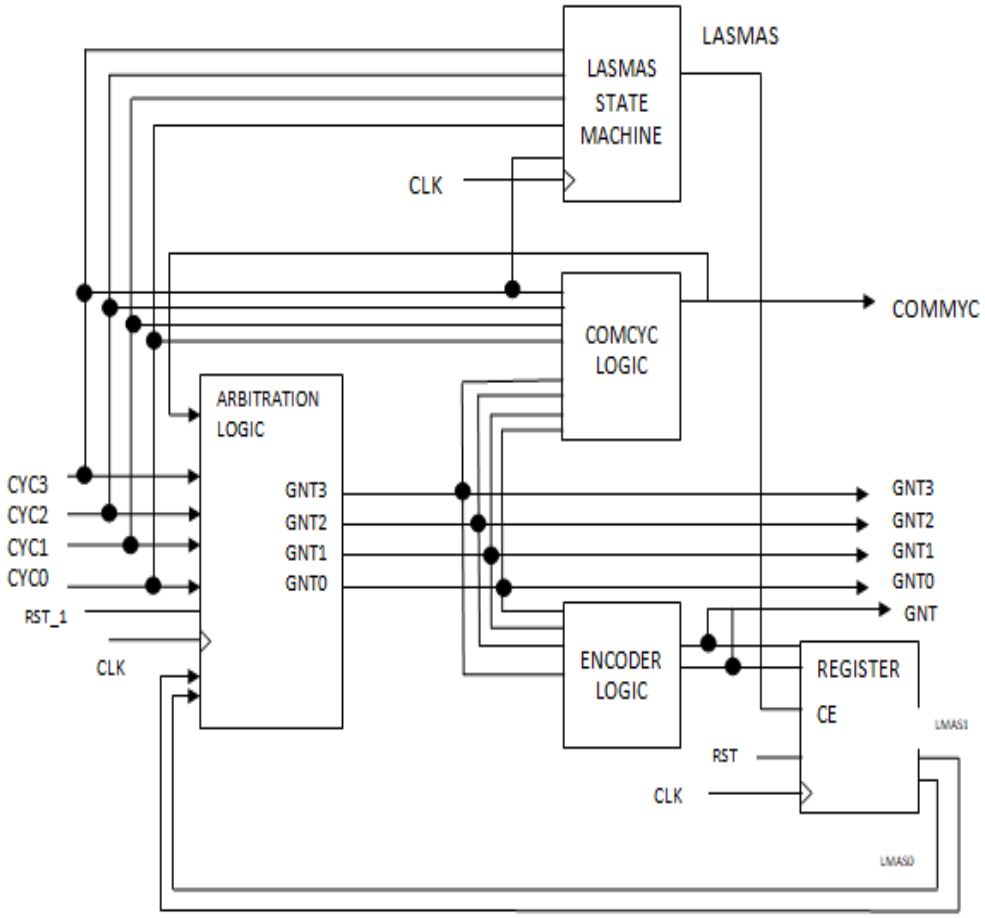

Fig. 2: Round robin arbiter block diagram.

The round- robin arbiter has maintained the history of the previous level master and from this level it is easy to find which master level accessed. The position of the grant signal GNT (1...0) will be retrieved by a register. The status register that catches a grant level will be decided with help of the output of LASMAS state machine. The level1 master denies CYC1 at a clock pulse if the master1 was access the bus. As a result COMCYC is denying the initiation of arbitration. The round-robin arbiter allows the bus to the second level of Master1 which is nothing but master2, because in the round robin master2 is next to the master1. The round-robin arbiter will be selected for cause of shared bus interconnection.SOC configuration requires a standard bus interface for IP centers to interact with one another. There exist numerous different transport interfaces, however AMBA, Core Connect and WISHBONE are notable and very much utilized SOC bus models. Each of the three bus models are open bus designs, which require no charges or eminences to utilize them. WISHBONE has more benefits contrasted with AMBA and Core Connect.

All the designers utilizing WISHBONE bus interface are permitted to transfer their structure in Open Core site where there exists numerous IP cores that help WISHBONE transport interface and they are for the most part allowed to utilize. So relying on the design details the designer can choose the IP cores from the site and paste them to the WISHBONE bus design to plan the last SoC. Contrasting the design of these three buses, it is seen that all are accessed by multiplexer interconnections. WISHBONE encourages variable interconnection and variable time details. This will be coded utilizing any hardware depiction language like VHDL and Verilog.

III. RESULT

Table 1: Performance Comparison of Lasmas and Existed Systems

Parameter	Existed System	Lasmas
MOSFETs	80	70

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MOSFET Generics	56	48
Boundary Nodes	156	149
Total Nodes	187	163
Accuracy (%)	91	98
Delay (ns)	58	39

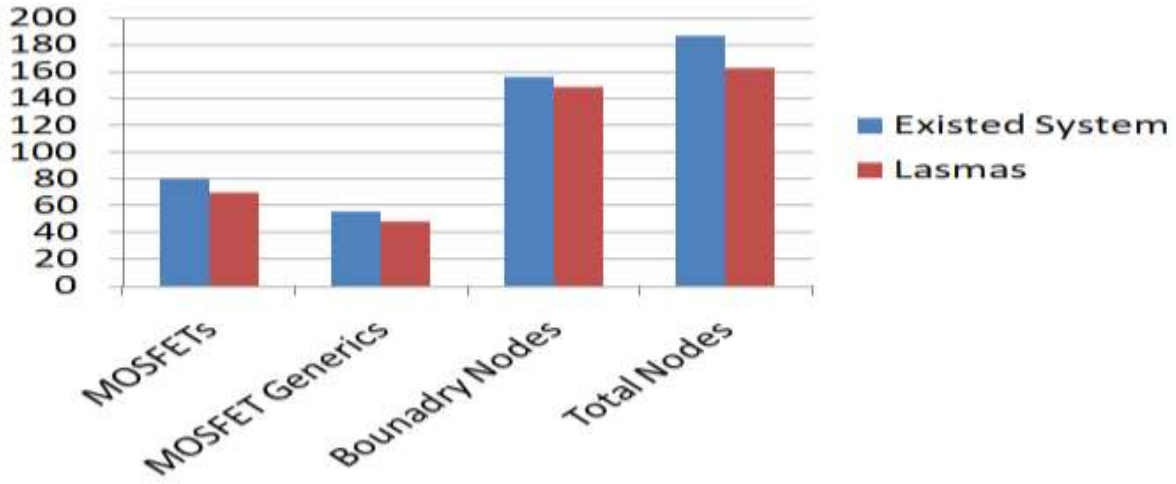

Fig. 3: Performance Comparison between Existed System and Lasmas

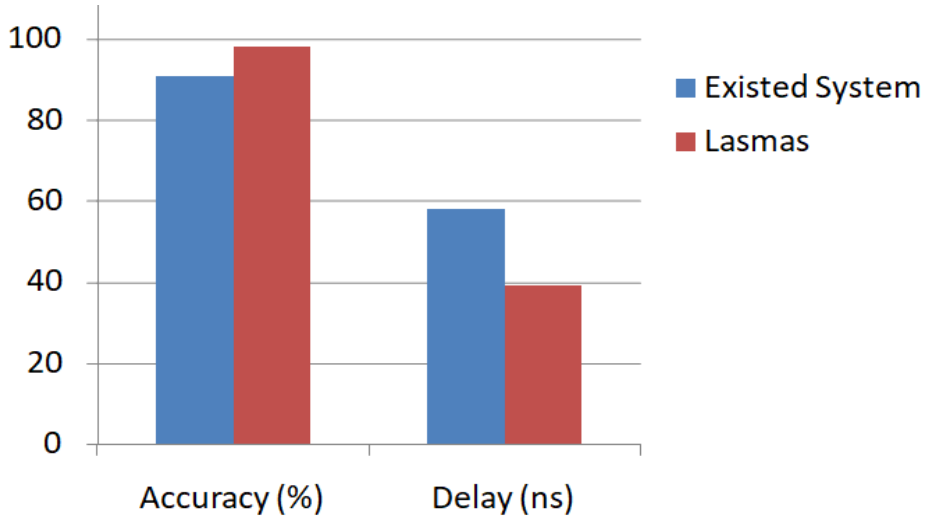

Fig 4. The accuracy and Delay for Existed System and Lasmas.

To completely make use of the data level parallel computing of TTA-DSP architecture, some DSP kernel algorithms in assembly code are transcribed. It is very complicated function that to perform the entire processing multimedia on the two cores, so this work is going on. So in this paper it was possible to give simulation based results of a TTA-DSP. Various required or useful parameters which are much useful to define the design performance this lasmas architecture can placed in Table I. All these are predicted in the processing cycles.

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Fig. 3 describes performance comparisons between TTA-DSP and the Lasmas. The consequences of TTA-DSP are getting by simulator, and the results of Lasmas are derived by advancement condition. All the 6 benchmarks are chosen from Lasmas DSP library. The results of simulator indicated that the exhibition of our proposed TTA-DSP processor is attractive than that of the current well known DSP processors for different standards, particularly for the algorithms which consists of trigonometric calculations. The performance is additionally far superior to that of the present embedded processor. The comparison among various parameters like accuracy, boundary nodes, delay and MOSFETs. Accuracy was increased in present LASMAS system. The delay, MOSFETs, MOSFET generics and boundary nodes are decreased in LASMAS system over an existed system.

IV. CONCLUSION

On a single chip it can design two processor cores and different interfaces to restrict a bus known as 128-bit ARM advanced microcontroller bus architecture AMBA. The output of the Lasmas state machine determines when the register grants the latch level. The development of transformational tasks with better accuracy and regular behavior can be implemented by DSP (digital signal processing) core. The dual-core embedded System-on-Chip (SoC) has used especially in high processing demands such as video processing, audio processing and sometimes mixing of both audio processing and video processing. The Transport Triggered Architecture (TTA) is used to design a DSP core which can minimize the hardware complexity, increase the flexibility and reduce the market time to a greater extent. The DSP design can be enhanced to a great extent by executing all these tasks. This is also effectively used as workloads in multimedia signal processing applications. This system was given optimum performance at suitable operating frequency. This technique has consumed very less amount of power. In this paper the design and implementation of dual logic Lasmas state machine for SoC has implemented using TTA-DSP architecture.

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