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LOW POWER DESIGN STRATEGIES ON FORCED LECTOR STACK TECHNIQUE IN VLSI CIRCUITS

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ABSTRACT: In the present era of Very Large Scale Integration (VLSI) technology low power plays a vital role. The scaling of threshold voltage in CMOS circuits results an increase in sub-threshold leakage current. Leakage current has become a major factor in total power dissipation of integrated circuits. This leakage current is reduced by introducing a forced lector stack technique for a CMOS circuits in this paper. The proposed method of forced lector stack technique can be implemented with the supply voltage of sub-threshold Voltage for designing CMOS gates in order to reduce the leakage current in active mode and standby mode without compromising the dynamic power dissipiation and reduce the delay at the same time. In addition optimization techniques of power dissipiation at different levels of abstraction are presented in this paper. The simulation results show the analysis of proposed forced lector stack technique circuit.

KEYWORDS: Dynamic power dissipation, Sub threshold leakage current, VLSI technology and Forced lector stack technique.

I. INTRODUCTION

The actual experiment on VLSI in the last decades concentrates on the performance, area, cost and power consumption. Recently this has been in progressed to change in any case and consequently power consumption is almost equal to the power required for area and speed consideration. For a circuit to circuit and application to application, the idea of reducing power consumption is varied. The main objective, in the field of application of small scale integrated circuits such as mobile phones is to maintain the lifetime battery, low weight and low designing cost. The business of semiconductors has been enabled by the scaling of CMOS devices in order to meet the demand of high performance and high synchronization density. However, when the component measurement becomes significantly smaller it generates a leakage current below the sub-threshold in a given short forwarded lengths which expands when turned off by a transistor. The transistors do not completely turned off. This was the other reason for the expanded sub-threshold leakage current. Therefore, for the innovations of silicon devices, the leakage power dissipiation plays a vital role for a considering a total power consumption. Area, speed and power are the three kinds of parameters to be considered. The dynamic, static and short-circuit are the generally three main factors for the cause of power dissipiation in VLSI CMOS circuits. Some developed methods and techniques are proposed to reduce the leakage current.

A key aspect of the configuration of the VLSI CMOS circuit is to reduce power dissipation by maintaining the better performance of the circuit. Hence for these purpose of maintaining the performance of circuit it must be required to scaling the threshold voltage. For the VLSI circuit designing, power consumption is turned into a major problem. Therefore, configuration of versatile framework performs an actual experiment by the use of outlined developments for reducing the power consumption in coordinated circuits. Scientists have proposed a variety of approaches to solve the problem of power consumption. There is no influence to meet trade-off among the area, power and speed in any case. It must be required to select suitable systems that meet application and objective requirements.

Finally, there are no battery-powered frameworks for the better performance, e.g. set-beat Personal computers and interactive media computerized flag processors. Reducing the cost of framework (cooling, grouping and use of vitality) is the general objective for minimizing the power while ensuring everlasting power stability of devices. These various requirements affect how the power improvement is managed and how much the designer negotiates on cost or performance for reducing power dissipiation. The advantage of design technologies with a low power is much more important than before. The main concerns in those technologies are area, cost and performance of design. Power consumption is simply a second problem.

The portable medical devices, laptops and wireless applications are some of the aggressive market sectors and the improvement in such sectors has recognized that power loss is of highest importance. The improvement in this critical market sectors such as wireless applications, laptops and mobile medical devices considers energy

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dissipation essential today. The measures to minimize energy consumption varied from one application to another application. Keeping the life time of batteries and decreasing the packaging price is important for the micro-powered mobile battery applications such as cell phones. In portable computers like laptops, only two parts of total power dissipation reduce the energy dissipation of the elements of the system's natural philosophy. After all, in high performance systems, process technology was the first factor to be directed in such designs.

II. POWER DISSIPATION AND CONTROL OF LEAKAGE POWER DISSIPATION

Generally, within a part of circuit power consumed is regarded as a power/MHz when limitation of a circuit is considered as power consumption. There is a major problem of high power consumption in a VLSI circuits since there is no steady state current during operation. Even though circuit may have low average power, the device may be collapse due to the voltage drops and electrical variations. Therefore average power consumption expression is as follows:

$$P_{avg} = P_{dynamic} + P_{short} + P_{leakage} + P_{static}$$

A. Dynamic power dissipation

According to the circuit supply voltage, timing of output capacitance and activity, this dynamic power dissipiation is in turn categorized into three types such as switched power dissipiation, short-circuited power dissipiation and glitch power dissipation. Occurrence of this leads the output capacity to charge and discharge which was mandatory for the transfer of information to the CMOS.

B. Static power dissipation

The power consumed in the circuit while there is no activity is called as Static power. The discharge currents of reverse bias diodes and sub thresholds are required for the static power dissipation. Because of sub-threshold discharge power collection, the sub-threshold discharge is recognized as an attractive one. Transistors do not turn off, only at the weak reversal of threshold voltage. The lust supports the threshold voltage which results a threshold current.

C. Short-circuited power dissipation

The shot circuited power dissipiation in a CMOS logic circuit is resulted by the change of logic state when the P-type and N-type are shorted for a while temporarily. For this circuit, current is not a reason to charge the capacitance which is called as short-circuited current consumption. It often occurs when the rise and fall time of the input signal is high or the output load capacity is low.

D. Leakage power dissipation

A system in the standby mode only, the leakage power dissipation occurs. Sub-threshold leakages, n-well leakages, gate leakages etc. are the various existed sources for discharge currents. VLSI-CMOS circuits set the processing parameters and CMOS logic gates have generally been used. It consists of various circuits in the case of a chip which have a direct current path between the power supply and the earth, so that it is examined with a static power component. Even though the sub-threshold discharge is a critical component in more than all above 130 nm technologies, the discharge current is constant and dynamic power is changing. Therefore the normal total power consumption is based on the Dynamic power consumption, Short-circuited power consumption, Leakage power consumption and static power consumption.

The leakage power dissipation is controlled by various methods that are proposed in the literature. In which one of the proposed method to reduce the leakage power is power gating that cut OFF the supply voltage consecutively turn off the device. In addition, between the path of source voltage and ground this technique uses a sleep transistor of large NMOS and/or PMOS transistors. Through this process the fundamental power and ground rail are formed in the circuit. If the circuit is operated in an active mode then it forms a negative effect. The Circuit requirement of area is increased with a sleep signal that provided by the use of additional hardware. The leakage power reduction process uses a method of smallest leakage vector which integrates both sleep transistors and the stacking effects. At a point of smallest probable leakage current in a circuit, input vector is calculated. It is required to use special purpose latches for this technique to increase the area. A method is described to reduce the leakage current called “Multiple threshold CMOS (MTCMOS)”. In this method sleep transistors with a high threshold voltages is used to provide low leakage current and low threshold transistors for logic are used to get a high performance of circuit. It has a complex process of depositing two oxides with different thicknesses which may results in total failure of gate or reduction of noise margin in a worst case. A method of Dual threshold is different from MTCMOS method. It maintains a steady state threshold voltage throughout active mode in this method and leakage currents are reduced in standby mode by the result of increasing the threshold voltage.

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III. FORCED LECTOR STACK TECHNIQUE

The major component of leakage current in a circuit is a sub-threshold leakage current. Generally, if the gate voltage (V_{GS}) is lower the threshold voltage of V_{TH} then current leakage in the way of drain to source is called as Sub-threshold or weak inversion conduction current. Following equation (1) represents the expression for sub-threshold leakage with related parameters of the device.

$$I_{SUB} = I_0 e^{\frac{V_{GS}-V_{TH0}-\eta V_{DS}+\gamma V_{SB}}{nV_T}}\left(1 - e^{\frac{-V_{DS}}{V_T}}\right) \quad \text{--- (1)}$$

$$I_0 = \mu C_{OX}\left(\frac{W}{L}\right)V_{re^{1.8}}^2 \quad \text{--- (2)}$$

$$V_r = \frac{KT}{q} \quad \text{--- (3)}$$

Here, in the above equations γ, η and n respectively indicates the coefficients of body effect, drain induced barrier lowering (DIBL) and slope shape factor sub-threshold swing coefficient. μ and C_{OX} indicates the carrier mobility and gate oxide capacitance respectively. In addition, $\frac{W}{L}$ indicates width to length ratio, K represents Boltzman constant, T indicates absolute temperature and q represents electron charge.

A. Stack technique

An approach of stack technique reduces the leakage power based on the stacking characteristics of MOSFETs which helps in reducing of leakage current. There is a cause of decrease in sub-threshold leakage current by the commencement of turning ON/OFF tendency between the two transistors at a point when that two transistors connected in a circuit are mutually executed. The restriction on performance of circuit is significantly differ by the increase of isolated transistors.

A development in the approach of stack technique is a Forced stack Technique in which two or more transistors connected in series which were turned off to reduce the leakage current further. The sub-threshold leakage depends on the total four terminal voltages. Since the V_{GS} reduces, I_{SUB} decreases exponentially when the input is grounded and the threshold voltage increases due to the body effect, the I_{SUB} dependency is used by the Stack effect. If there is an increase in threshold voltage, a decrease is observed in DIBL coefficient that reduces the leakage further.

B. Lector technique

The circuit of Lector technique approach has a p-type leakage transistor and an n-type Lector Transistor (LCT) connected between the pull-up and pull-down stages of a logic gate. The source of one LCT controls the gate terminal of another LCT. Hence any one of the LCT is constantly operated in its near cutoff region because of the above circuit arrangement. The state in which transistors with more than one number turned OFF in a path between supply voltage and ground is much low leaky compared to the state in which only one transistor turned OFF in a path between ground and power is the main idea of this LECTOR circuit. The standby current of the circuit at which deep submicron transistor operated under a sub-threshold region is exponentially changed with respect to the gate-source voltage. The series combination and parallel combination of MOS transistors are involved in the design of almost CMOS logic circuits. The sum of every one of parallel connected transistors current is computed as those MOS transistors direct current (DC). The calculation of leakage current is typical for transistors connected in series because of nonlinear properties of them. The analysis of stacking current of transistors when they are operated in sub-threshold region is as followed:

$$I_{s1}: I_{s2}: I_{s3} = 1.8\ exp\left(\frac{\eta V_{DD}}{\eta V_T}\right):1.8:1$$

Where I_{s1} (i=1, 2, 3) indicates the leakage current for stacked MOS transistors.

C. Forced Lector Stack Technique

This approach of Forced Lector stack technique is derived from the both approaches of forced stack and lector techniques. The fundamental thought of implementing Forced Lector stacked technique is that minimizing the staking current of transistors effectively in a path between supply voltage and ground that results in minimization in leakage current is employed with the less number of transistors. In this technique, compared to a state in which only one transistor is turned OFF in a path between supply voltage and ground, a state in which more than one transistor is turned OFF in a path between supply voltage and ground has affected little. The Schematic

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diagram of a forced lector stack circuit is shown in figure (1). The two Leakage power control transistors such as LCT are connected to the nodes N1 and N2 and the source voltage of one LCT controls the gate terminal of another LCT.

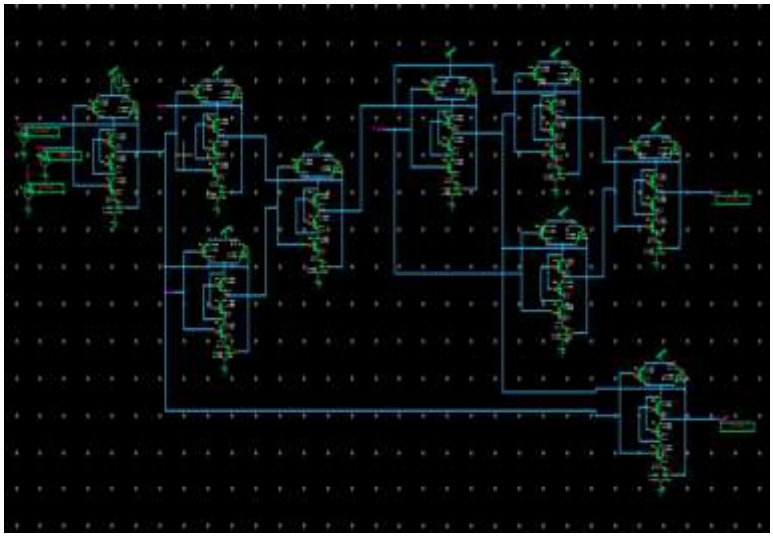

Fig. 1: Schematic of Forced Lector Stack Circuit

Those LCTs are known as self controlled stacked transistors. Therefore any external circuit is not required since the LCTs are self controlled. Then the limitation with the quiescent transistor system was overcome in this way. The leakage current decreases when the LCT current develops an opposition in a path between supply voltage V_{DD} and ground. The two LCTs which were used in this technique are connected at a inputs of CMOS, i.e. NMOS is connected to the pull down stage where as PMOS is connected to the pull up stage. Hence, the gate terminal of PMOS LCT is controlled by the source of the NMOS LCT and NMOS LCT is controlled by the source of the PMOS LCT. As a result, one of the LCTs is always operating close to its cutoff region for contributing input to the CMOS. This provides additional resistance on the path between supply voltage and ground, which consequently reduces the sub threshold leakage current and therefore the static power.

D. Optimization Techniques at Abstraction Layers

The below described layers are the abstraction layers of a CMOS circuit design. The power optimization techniques are implanted in each of these abstraction layers that are described as follows.

System level: A system is reconfigured dynamically with a less quantity of active components or a minimum load by a design methodology of Dynamic Power Management which offers a higher level of performance. This can be achieved in the system by employing power manageable components that shows an impact on the total power consumption of the circuit. Power is measured only at the circuit level or gate level with the help of power analysis tools.

Algorithm level: Behavioural synthesis optimizes the circuit size for the low power. This optimization of circuit by the behavioral synthesis includes the optimization of overall utilized algorithm which depends on components used in the circuit. From the high level specification problem only, it denotes the register transfer level design. Better algorithm should be employed to reduce the usage of hardware.

Architectural level: The pipelining and parallel processing are the two techniques involved in the architectural level. The clock speed is increased or power consumption is reduced in the pipelining process where as area and power dissipiation are minimized in the parallel processing. The circuit operation speed is also enhanced by this.

Circuit level: Every transistor size is adjusted to get a minimum power in this basic circuit level. The optimization of circuit decreases the area that consequences to a smaller area. Delay of transistors in the circuit is increased when the size of transistors or number of transistors in a specified gate are increased. Then the fan-in gate's delay increases as load capacitance increases. Therefore, since the load capacitance increased, overall delay of the circuit also increased.

Technology level: This is a different from the CMOS technologies which optimizes the power or delay by the multiple threshold voltages of transistors. If a substrate of the semiconductor device and insulating layer are connected then at this interface an inversion layer formed at which the gate voltage is obtained as a threshold voltage of a MOS. An important delay method for attenuating the clock period is obtained by the square

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measurement of low-threshold voltage devices which has a faster switch rate. Significantly there is a high static leakage power in the low power devices.

The square measure of high voltage threshold devices is used in non-critical processes to reduce static leakage power without incurring a delay penalty. Compared to the low threshold devices, static leakage power is typically reduced by ten times in the high threshold devices.

IV. RESULTS

Simulation on the proposed technique of forced lector stack circuit is carried out through the Tanner EDA (Exploratory Data Analysis) tool in a standard CMOS technology of 250nm (nanometer) as shown in Figure (2). To this standard CMOS technology of 250nm, parameters of Berkeley Predictive Technology in BSIM3 model are used. By using the random input vectors, Dynamic power is deliberated and the average power dissipation is calculated in a cyclic period of 200ns through Tanner EDA tool. A supply voltage of 0.5v is applied to the circuit and then V (a) and V (b) are varied to threshold voltage which was considered by the tanner tool for measuring the sub threshold leakage current and V(c) is varied to dc source by the supply voltage. Thereby measure the Average current for the duration of 200ns. The values of threshold voltages considered by the simulation tool are 0.55 and 0.5V for both PMOS and NMOS transistors respectively. Also the width to length ratio of NMOS and PMOS is considered to be 3.

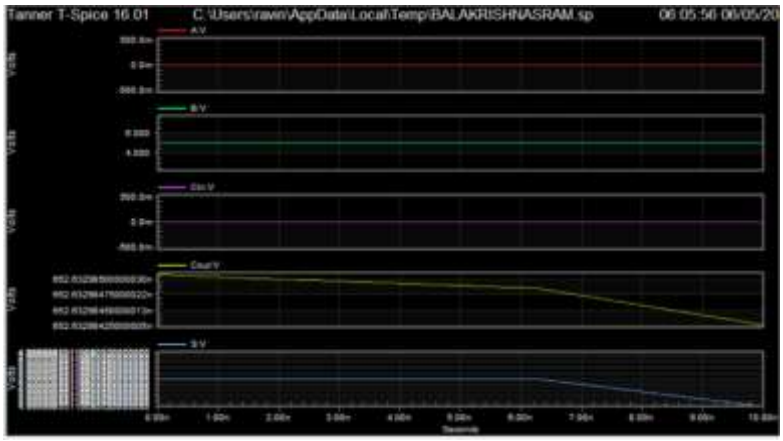

Fig. 2: Output Waveforms

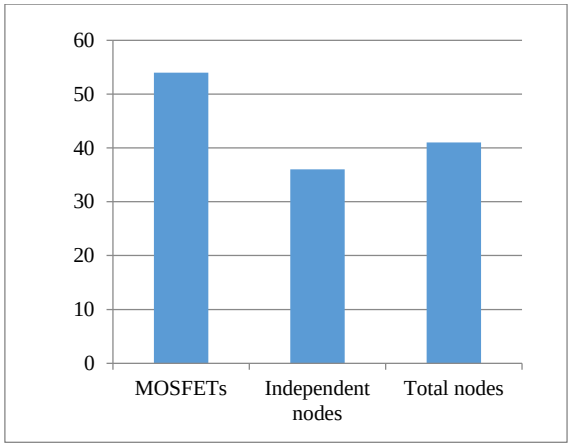

Fig. 3: Node Count of Forced Lector Stack Circuit

The leakage power is measured by using the Tanner T-SPICE simulator and simulation is performed with a 250nm process parameters. Then by using the same set of random vectors used in the above case, both the transistor circuits of stacked based gate and lector based gates are excited to measure the Leakage power dissipation. The circuit must have to wait for long period before exciting with another set of input vectors which are enough to decrease the activity of circuit switching after which the power is dissipated as a result of the leakage currents. The below table (1) shows the Time delays of forced lector stack based CMOS circuit. These delay characteristics are shown in figure (4) and figure (5).

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Table 1: Time Delays of Forced Lector Stack Circuit

SI.NO	Parameter	Delay
1	Parsing	0.21 sec
2	Setup	0.09 sec
3	DC operating point	0.59 sec
4	Transient Analysis	0.02 sec

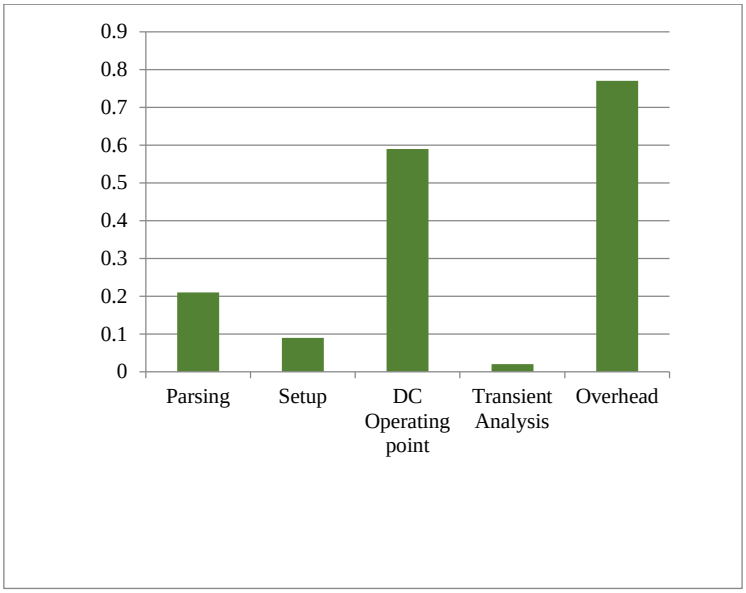

Fig. 4: Delay Characteristics

The design of low voltage circuits leads to a low leakage power. Since the sub-threshold leakage power gets to be distinctly good to power consumption dealing with the leakage power is an incredible test in nanometer scale innovations.

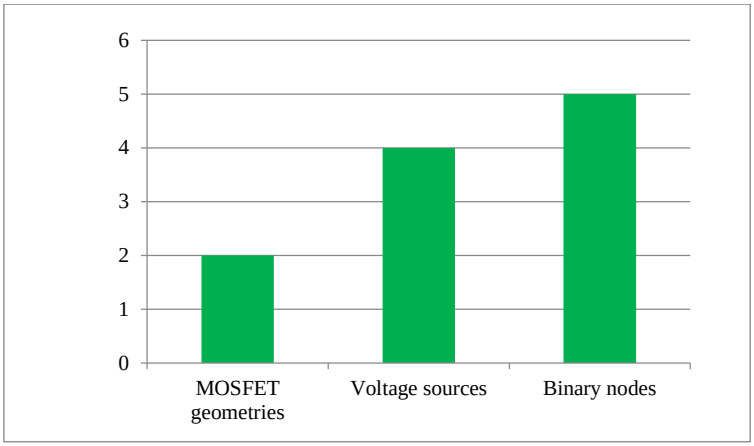

Fig. 5: Geometric Parameters of Forced Lector Stack Circuit

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V. CONCLUSION

The main idea behind the proposed circuit is decreasing of leakage power dissipiation by increasing the stacking of transistors then the systematic analysis of Forced lector Stack based circuit is presented in this paper. The advantage of the proposed circuit is that it does not affect dynamic performance because it does not require additional power supply and verification circuits. Therefore without increasing the dynamic power dissipation, this technique offers an approach to reduce the leakage power dissipation.

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