JOURNAL OF CRITICAL REVIEWS

ISSN- 2394-5125 VOL 7, ISSUE 15, 2020

DESIGN AND IMPLEMENTATION OF LOGIC OPERATIONS AND ALU WITH LOW DELAY PROFILE USING REVERSIBLE GATES

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Received: 14 March 2020 Revised and Accepted: 8 July 2020

ABSTRACT: Basically, reversible logic gates are most commonly used in the applications of CMOS, SOC, VLSI and DSP to reduce the energy consumption. Mainly reversible logic gates use the one to one mapping technique. In this paper the design and implementation of logical operations and ALU using reversible gates are presented. Reversible gates generally use ancillary inputs to generate function of gate. In this system firstly logical and shifting operations are performed. The shifting operation performed in parallel form from right shift and left shift. In this paper design the ALU using DKG gate,DPG gate and TOFFOLI gtaes. By using these gates we achieved the effective results in terms of route delay, logic delay and total delay.

KEY WORDS: Reversible logic, Reversible gates, DKG GATE, DNG Gate, Toffoli Gate.

I. INTRODUCTION

The PC gadgets are these days an indispensable piece of a human's life. The advancement of the framework is likewise developing as innovation advances. This offers ascend to expanded of energy, which is large issue confronting the world today. In year 1960,landauer exhibited vitality dispersal because of data misfortune in high innovation circuits and frameworks planned utilizing irreversible equipment .the loss of the slightest bit of data lost would disseminate ktln2 joules of vitality as per the Lindauer's guideline where k is the steady of the Boltzmann ,T is the outright temperature.

In 1973,bennett showed that it must be built from reversible circuits to forestall ktln2 joules of vitality scattering in a circuit. Reversible circuits have a similar number of inpunts yields and there is balanced planning among information and yield vectors. Thus, the info state vector can generally be figured particularly from the yield state vector.
Using the System on chip, the design is constructed on the Chip designs and they occupy the chip less area and improving both the yield cost. If delay cells of even numbers are used, it will generate both in the quadrature phase outputs and phase. Because of their low quality factor the phase-noise performance of system on chip is poor. In the System on chip basic element is a cell of a Dependability Manager. The complementary pairs of positive channel of metal oxide and negative channel of metal oxide consist by the cell. The complex circuit behavior is by estimated and determined by the results of obtained Dependability Manager (DM) [4].

Using the technology of complementary metal oxide of semi conductor all the digital and the designs of analog can be fabricated. In the gain stages a system on chip, is connected to a loop from the last of the output stage and it is given to the input of first stage. The system on chip has been designed for different stages. Because of the various advantages.

CMOS methodology is the most preferred techniques in VLSI designs. Power dissipation will be accomplished if there is charging and discharging in a capacitor. The amount of energy = ½ CV2 will be lost every time when the capacitor goes to ground. This behavior of capacitor will leads to reduce the power consumption in VLSI circuits. In the last few decades the technology called integrated circuit needs to develop a circuit with a low power consumption in a VLSI circuits. The IC technology is very useful in portable devices ,power amplifiers and radio receivers In this technology several transistors are fabricated on a single chip , which enables the performance of system to a better extent. Hence low power consumption , area and delay, will be achieved in a better way in a VLSI circuits by implementing the concept of clock gating with a adiabatic logic circuit at a low cost.

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The system on chip of different stages has been designed by using the technology of complementary metal oxide of semi conductor employed tool. There are 5-stages of System on chip it is large in to the output of the stage one and it is fed into the next stage of input and finally it is feedback in to the output and the input of the first stage. The voltage supply is also sufficient and it should be given and reset in the voltage of input and it is applied at once to the circuit, so it spontaneously arise the oscillations. Where the positive channel of metal oxide of semi conductor which is also called as the network of pull-up and the negative channel of metal oxide of semi conductor also called as the network of pull-down.

Arithmetic and Logic Unit (ALU) is the microchip workhorse and characterizes processor working velocity. Both current processors give independent equipment to standard number juggling tasks calculation. Notwithstanding quick number juggling equipment, processors are regularly fitted with on-chip memory (store) to accomplish generous enhancements in execution by dispensing with delay because of fundamental memory information get to.

The principle objective of this work is to examine reasonable square structure. The most basic part in the plan of advanced frameworks is an Arithmetic Logical Unit. It is a necessary piece of a PC processor that plays out its arithmetic and logic unit activities just as a mix rationale unit. In Very Large Scale Integrated Circuit (VLSI) from processors to application-specific Integrated circuits circuits (ASICs), ALUs of various fixed piece widths and full accuracy bit-width are regularly required.

The ALU (Arithmetic Logic Unit) is essentially the core of a CPU. This permits the machine to include, erase and perform basic consistent activities like AND, OR and so forth. Since each machine requires such essential capacities to have the option to do, they are regularly remembered for a CPU. An ALU is a circuit of mix rationale which can have at least one source of info and just one yield. The yield of ALU relies entirely upon inputs that are applied as a component of time at that point, and not on past conditions. A straightforward ALU in its essential structure is comprised of two operand inputs, one contribution to pick the ideal activity and one yield to the outcome. ALU 's unpredictability will shift starting with one processor then onto the next. In the current work is manufactured 32 piece ALU with 16 activities.

Section II deals with the reversible basic gates, section III.literature survey. IV.shows the proposed 32-bit ALU designs, respectively. Section V discusses conclusions and responses. Finally, section IV presents the conclusion.

II. REVERSIBLE GATES

A logic gate with same number of sources of info and yields n × k rationale gadget where n and k is the quantity of data sources and yields with coordinated planning is called reversible logic gate. In this rationale gate number of yield ought to be equivalent to that of sources of info (for example n = k). A gate is called reversible if the info will be remarkably recouped from yield and there ought to be coordinated correspondence between the information and yield rationale. To plan a reversible rationale circuit a gathering of reversible rationale gates are required. A reversible rationale gate ought to have following highlights.

- In the circuit number of output should be equal to number of inputs.
- NOT gate is a reversible gate with one output and one input.
- Minimum input constants.
- Minimum reversible gates.
- Minimum garbage outputs.
- Minimum hardware complexity.
- The cascading gates length should be minimum.
- No feedback is provided.

The expense of accessible every single crude gate is Quantum cost. The quantity of crude reversible rationale gates required to plan an advanced circuit will chooses the quantum cost. Trash yield is the undesired yield of a reversible gate. In this plan idea, the reversible gate yield can be utilized neither as an essential yield nor as contribution to different gates Always its obligatory to keep up equivalent number of information sources and yields by including either info or yield dependent on condition.

In future developing advancements, for example, quantum computing, optical computing just as ultra low-power VLSI circuits, DNA processing has extensive applications to accomplish zero-power scattering under perfect conditions. Reversible rationale is significant for building low-power low-misfortune computational structures that are exceptionally basic for building math circuits utilized in quantum registering, nanotechnology, and other low-influence computerized circuits. A few scientists have as of late cantered their endeavours around planning

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and integrating proficient, reversible rationale circuits. Frequently utilized in thermodynamics and adiabatic CMOS are reversible usage.

The VLSI circuits which uses reversible logic to achieve low power dissipations adiabatic logic. This logic can helps in reducing energy loss during the capacitor behavior. The charge recovery can mainly achieved by using this logic. The required power can be reduced in this logic by retrieve the stored energy to a back in a VLSI circuits during the switching operations. Any circuit should meet two requirements or conditions to fulfill adiabatic function.

They are
If there is a voltage across a transistor then never don't do switch on
If there is current flowing through a transistor then never don't do switch off. The below figure (1) shows the Feynman gate. Here A and B are the inputs and P and Q are the outputs. The quantum cost of Feynman gate is 1.

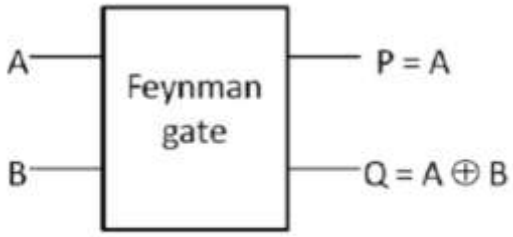

Fig. 1: FEYNMAN GATE

The below figure (2) shows the toffoli gate. Here a, b and c are the inputs.

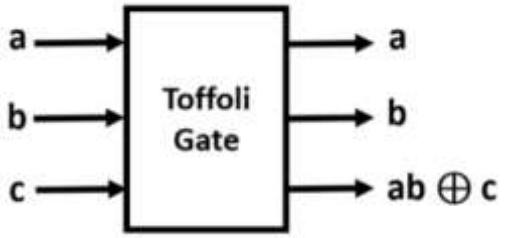

Fig. 2: TOFFOLI GATE

The below figure (3) shows the Fredkin gate. In this A, B, C are the inputs and P, Q, R are the outputs.

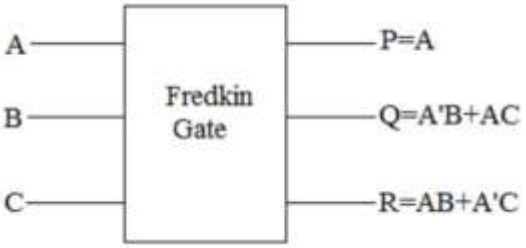

Fig. 3: FREDKIN GATE

III. LITERATURE SURVEY

In 2010 Lihui Ni et.al introduced a general method of building the complete reversible adder. This method uses only two reversible gates and two garbage output for Designing the adders.

In 2015Mandeep Kaur and Chakshu Goel developed a reversible multiplier that was efficient in terms of quantum. Growing demand for power dissipation reduction in digital multipliers has led to new computation mode for multiplier design is reversible logic computing model.

In 2017, Dhoumendra Mandal et.al proposed a concept using reversible logic gates for all the optical one bit binary comparators. In this design reversible logic gates were used to construct a one-bit comparator based on frequency encoded data. You may use this comparator circuit to propose all optical Arithmetic Logic Units.
In our work we have proposed ALU with low delay profile using reversible logic gates.

Depending on the mode of operation Multi-threshold CMOS switches permits blocks to switch on or switch off. A power that is dissipated by a device when the transition takes place from logic 0 to logic 1 is called dynamic power. The dynamic power will be presented when there exists a change in dissipation of power in CMOS inverter. The clock frequency and applied voltage are directly proportional to the power.

Adiabatic Logic is mainly implemented to get low power and delay by using reversible logic. Some adiabatic logics are not that much effective or efficient mainly in terms of power consumption. Generally power consumption will be dependent with resistance of the charging path. A new logic family known as Improved PFAL (IPFAL) will be studied in this paper, where all n- and p channel circuits are exchanged hence the charge can be retrieved via n-channel MOSFET. This permits to reduce the charging path to a factor of 2, and it can produces a reasonable decrease of the energy consumption. Research work based on a 0.13µm process affirms the enhancements regarding power dissipation over a huge frequency range.

IV. LOGICAL OPERATIONS AND ALU USING REVERSIBLE GATES

The below figure (4) shows the block diagram of ALU based reversible gates. In this initially, two inputs are taken they are input-1, input-2. The both input 1 and input-2 perform logical operations. Shift register is used to save the value and it acts as a memory. Now all the obtained values are multiplier, adder and subtracted. All these values together form a final output. Hence there is no complexity in the system.

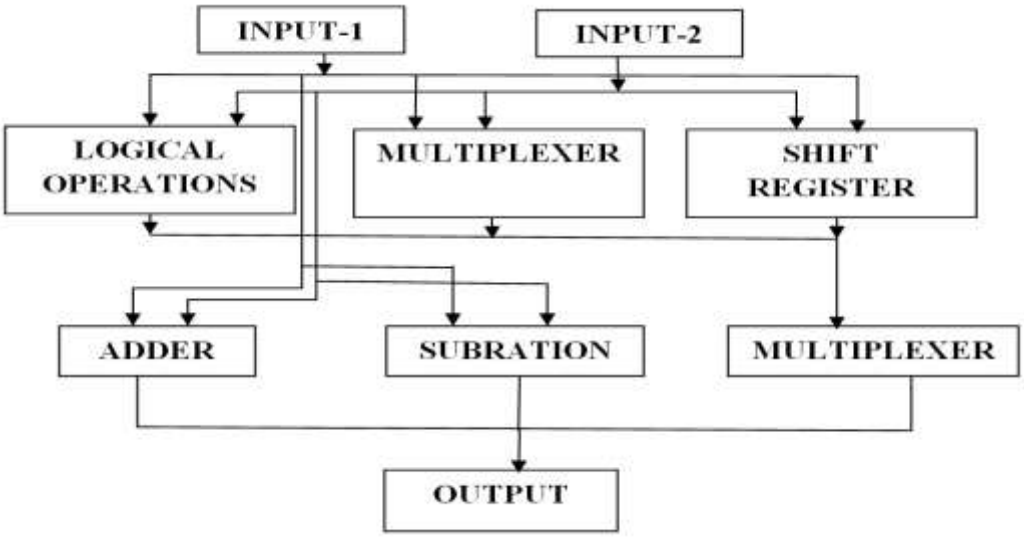

Fig.4: BLOCK DIAGRAM OF LOGICAL OPERATIONS AND ALU USING REVERSIBLE GATES

Logical activities incorporate any tasks that control Boolean qualities. Boolean qualities are either obvious or false. In settings where Boolean administrators are not blended in with numerical administrators.

In hardware, a multiplexer, otherwise called an information selector, is a gadget that chooses between a few simple or advanced info signals and advances it to a solitary yield line. A multiplexer of sources of info has select lines, which are utilized to choose which information line to send to the yield.

The Shift Register is such a progressive method of reasoning circuit that can be used for the limit or the trading of twofold data. This progressive device stacks the data present on its information sources and a short time later Shift s or "Move s" it to its yield once every clock cycle, along these lines the name Shift Register.

A move register in a general sense involves a couple of single piece "D-Type Data Latches", one for each data bit, either a method of reasoning "0" or a "1", related together in a successive sort daisy-chain strategy with the objective that the yield from one data lock transforms into the commitment of the accompanying snare, and so forth.

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V. RESULTS

The below figure (5) shows the RTL schematic of proposed system.

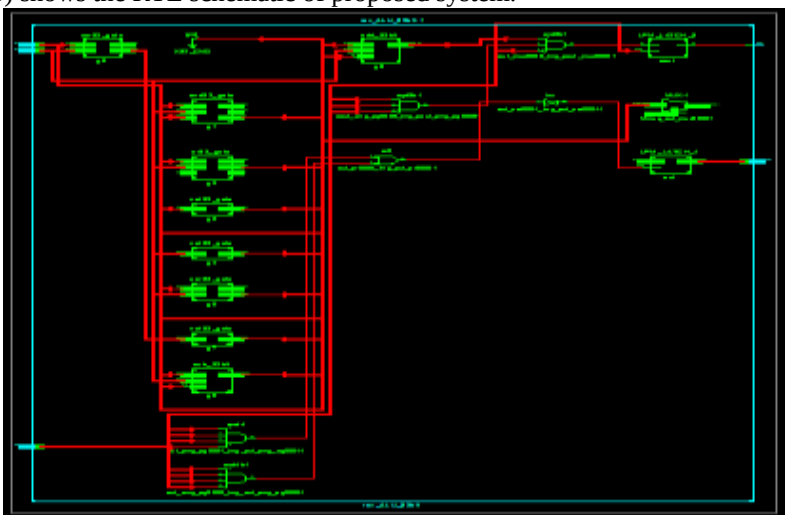

Fig. 5: RTL SCHEMATIC OF LOGICAL OPERATIONS AND ALU USING REVERSIBLE GATES

The below figure (6) shows the output waveform when logical operation is performed.

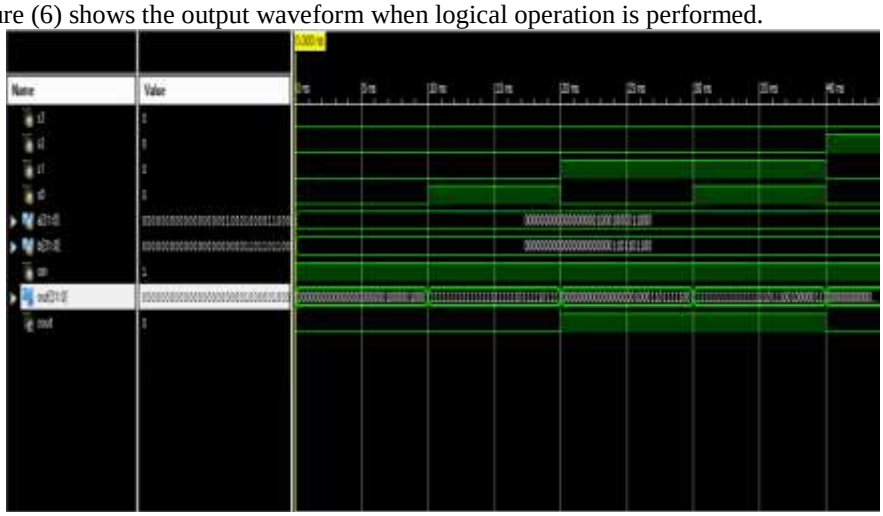

Fig. 6: OUTPUT WAVEFORM OF LOGICAL OPERATIONS

The below figure (7) shows the output waveform of Arithmetic operations
Of the system.

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Fig. 7: OUTPUT WAVEFORM-1

The below figure (8) shows the logic delay and route delay of proposed system.

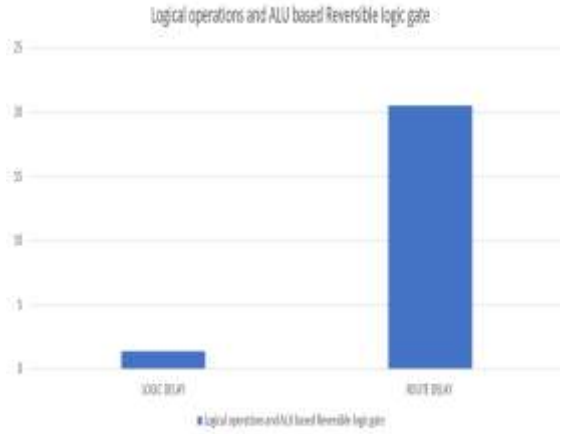

Fig. 8: LOGIC DELAY AND ROUTE DELAY OF PROPOSED SYSTEM

The below figure (9) shows the Total delay of proposed system.

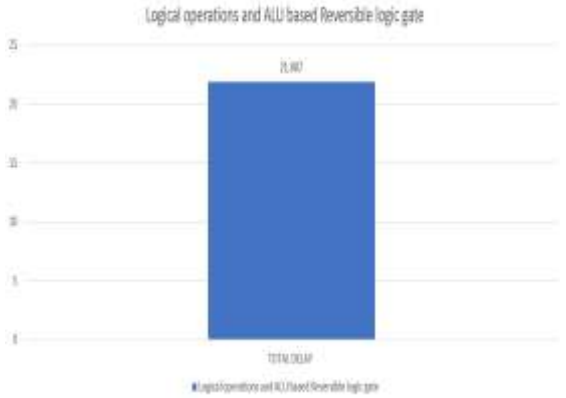

Fig. 9: TOTAL DELAY

VI. CONCLUSION

In our research work we have proposed ALU with low dealy profile using Reversible logic gates. In VLSI circuit the Power consumption was reduced using the reversible logic gate technique. This reversible logic has different applications such as communication, nano technology, computers and optical computing. This proposed method has many advantages compared with existing methods. In proposed 32-bit ALU using

reversible logic we reduced the total dealy by50%and levels of logic also reduced by 55% with the existing methods.

Parameter	Existing 32-bit ALU using reversible logic gates	Proposed 32-bit ALU using reversible logic gates
Delay	40.512ns	21.907ns
Levels of logic	67%	35%

VII.REFERENCES

[1]. Ismail Gassoumi, Lamjed Touil, Bouraoui Ouni, "Division Circuit Using Reversible Logic Gates", 978-1-5386-4449-2/18/$31.00 ©2018 IEEE.
[2]. Kirti Batish, Shruti Pathak, Raghav Gupta, "Comparative Analysis For Performance Evaluation Of Full Adders Using Reversible Logic Gates", 978-1-5386-6483-4/18/$31.00 ©2018 IEEE.
[3]. A.G.Rao, Dr. A. K. D. Dwivedi, "Design of ESOP-RPLA Array using DRG2 and DRG4 Gates based on Reversible Logic Technology", 978-1-5090-6170-9/16 $31.00 © 2016 IEEE.
[4]. A.G.Rao, A. K. D. Dwivedi, "New Multi-Functional DR Gates and its Application in Code Conversion", 978-1-4799-6042-2/14/$31.00 ©2014 IEEE.
[5]. Lenin Gopal, Nor Syahira Mohd Mahayadin, Adib Kabir Chowdhury, Alpha Agape Gopalai, Ashutosh Kumar Singh, "Design and Synthesis of Reversible Arithmetic and Logic Unit (ALU)", 978-1-4799-4555-9/14/$31.00 ©2014 IEEE.
[6]. Ankur Sarker , Avishek Bose , Shalini Gupta, "Design of a Compact Fault Tolerant Adder/Subtractor Circuits Using Parity Preserving Reversible Gates", 2014 17th International Conference on Computer and Information Technology (ICCIT).
[7]. A.G.Rao, Dr. A. K. D. Dwivedi , "Dr. A. K. D. Dwivedi, "Design of Multifunctional DR Gate and its Application in ALU Design", 014 13th International Conference on Information Technology.
[8]. Muskan Bhusal, Rohith R, Sakthivel R, "Single Bit Fault Detecting ALU Design using Reversible Gates", 2014 International Conference on Emerging Trends in Information Technology and Engineering (ic-ETITE).
[9]. Marek Szyprowski, "Reducing quantum cost in reversible Toffoli circuits", IEEE, 2013.
[10]. Raghava Garipelly, P.Madhu Kiran, A.Santhosh Kumar, "A Review on Reversible Logic Gates and their Implementation'', International Journal of Emerging Technology and Advanced Engineering, March 2013, Vol. No. 3, Issue No. 3.
[11]. W! David Pan and Mahesh Nalasani, "Reversible logic", 0278-6648/05/$20.00 © 2005 IEEE.
[12]. Mr. Devendra Goyal, Ms. Vidhi Sharma,"VHDL Implementation of Reversible Logic Gates", International Journal of Advanced Technology & Engineering Research (IJATER), 2004.

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