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4 TO 16 DECODER USING 2 TO 4 DECODER BASED ON FINFET IN 22NM TECHNOLOGY AND MTCMOS

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ABSTRACT- This paper introduces the need for higher performance applications with low power consumption as we see there is lots of difficulty in using low power devices for a higher rank application like microprocessor, DSP, SRAM. As we know the Decoder plays an important role in memory design & logical circuit design. In this paper, I have been comparing the parameter Power delay product, Energy delay product, Power consumption, and Delay on 14T and 15T based using 4-16 decoder base on MOS, FinFET, and FinFET using MTCMOS as proposed in 22nm technology. So the final proposed circuit is obtained by application of MTCMOS, to vary threshold from the ground path of the final 15T based on 4 to 16 decoder. where we get significant improvement in proposed work.

KEYWORD: Line Decoder, FinFET, MOS,MTCMOS, Threshold voltage ,EDP ,PDP, LTspice

I. INTRODUCTION

In VLSI technology, as we know that it contains thousands of transistors in a single chip called Integrated circuits (IC) with an increase in transistor densities by the law of Moore's, also increasing the power consumption with higher clock frequency. Now the trade occurs, where we try to make efficient logic circuits to optimize the key factors like Power loss, leakage current, voltage source, etc through which we can make the device more efficient with low power consumption.VLSI occupies a comparatively a low area. The size of the circuits is lessened. Discrete components use a lot of power. The authenticity in using VLSI in circuits is extremely high. The operating speed of components powerfully increasing. The inclusive cost of the device is now reduced. The employ of VLSI in Digital Signal Processing Commercial Electronics, Automobiles, medicine.CMOS devices have two basic elements static power utilization is low high noise immunity.[7] CMOS production does not waste much heat as other logic, like NMOS type logic or TTL which have a current level state, when not in changing state. That feature allows to CMOS merge a high substance of logic functions on a chip. So CMOS is the most broadly used technology to be in the appliance in VLSI chip design. Storage register combinational logic and the associated interconnection are very easy to design and implement in both NMOS and CMOS Poly-silicon resistance is the most common gate electrode and interlayer connect material in use today in the manufacture of VLSI MOS devices. Poly-silicon has many desirable properties including good etch ability, good oxidation characteristics, mechanical stability at high-temperature excellent step coverage, and adhesion. It's one major drawback is its relatively high resistance. VLSI layout design consists of creating appropriate masks that define the sizes and locations of sources, drains, gates, and the necessary interconnection. CMOS is widely used in VLSI circuits due to its high scalability, low power consumption, and high performance. With the help of the CMOS, the massive amount of combinational and sequential logic gates can be implemented for complex and high-speed computation purposes. One of the combination circuits which can be implemented using CMOS is Decoders.[3] So in this paper, I introduced decoder based on FinFET which compare to decoder based MOS in various parameter with respect to MOS where we will get the performance parameter results by using between two devices by using 22nm technology by using simulation software Hspice.

[A] Decoder

A line decoder is a basic unit of design for converting analog to digital conversion and vice versa and it is a combination of ‘n’ input line which gives to a maximum of 2^n output lines. This is mainly used for logical cicuits and data transfer [8]. We always try to improve our decoder design time to time according to circuit or application requirement, making it fast transmission by reducing the delay of the decoder When paired decoders

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have extra information or a greater number of bits. As we go on to higher logical design like memory based on the application we use Address decoder, which is a fundamental component in all SRAM memory square which reacts to extremely high recurrence. Access time and force utilization of recollections are to a great extent controlled by decoder plan [4]. Structure of irregular access memory (RAM) is commonly partitioned into two sections, the decoder, which is the hardware from the location contribution to the word line, and the sense and segment circuits, which incorporates the bit line to the information input/yield circuits. Because of the huge measure of capacity cells in recollections, it tends to be discovered different arrangements of address decoder plans prompting power utilization decrease and execution improvement. We estimate delay and power by using Hspice software.

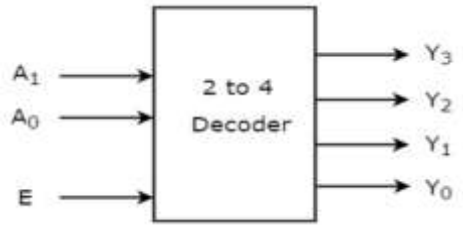

Figure 1: Symbol of 2 to 4 decoder

In figure 1,Realization of 2 to 4 Decoder has 2 inputs A_1 & A_0 and have a output 4 Y_3, Y_2, Y_1 & Y_0.

Table 1: Truth table of 2 to 4 decoder

E	A1	A0	Y3	Y2	Y1	Y0
0	X	X	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

One of these four outputs 1 will be for each input combination when enable, E is '1'.

[B] FinFET

FinFET transistor utilized in the structure of the current processor, kind of 3 dimensional. As in prior, planar structures, it is based on an SOI (silicon on separator) substrate. In any case, FinFET plans additionally utilize a leading channel that ascents over the degree of the encasing, making a slim silicon structure, formed like a blade, which is known as a gate anode. This blade formed cathode permits various gates to work on a solitary transistor. A blade field-impact transistor has multigate implements, a MOSFET based on a substrate where the gate is put on two, three, or four sides of the channel or folded over the channel, framing a two-fold gate structure [12]. The FinFET is a transistor which originate by Chenming Hu at Berkeley, which attempts to overcome the worst types of short-channel effects encountered by deep submicron transistors, such as drain-induced barrier lowering (DIBL). This structure is called the FinFET because its Si body resembles the back fin of a fish. An important FinFET characteristic is controllability of V_t (threshold voltage). [1] [9] (Fig. 2a)
FinFET is a promising alternative for watching out for the troubles exhibited by continued scaling. It is contraption includes a slim silicon body, the thickness of which is implied by TSi (thickness silicon body), wrapped by gate anodes [10]. The present streams corresponding to the wafer plane, while the channel is confined inverse to the plane of the wafer. In light of this explanation, the device is named semi planar. The free control of the front and back gates of the FinFET is practiced by drawing without end of the gate cathode at the most elevated purpose of the channel. Making of FinFETs is acceptable with that of normal CMOS, thusly making a possible exceptionally quick association to gathering. These devices come in various sorts. Firstly, The IG FinFET i.e. 4T, has two gates with excellent channel controlling capability, independently. This Offers different design approaches, like by using different input signals on channel gate make it independent gate mode

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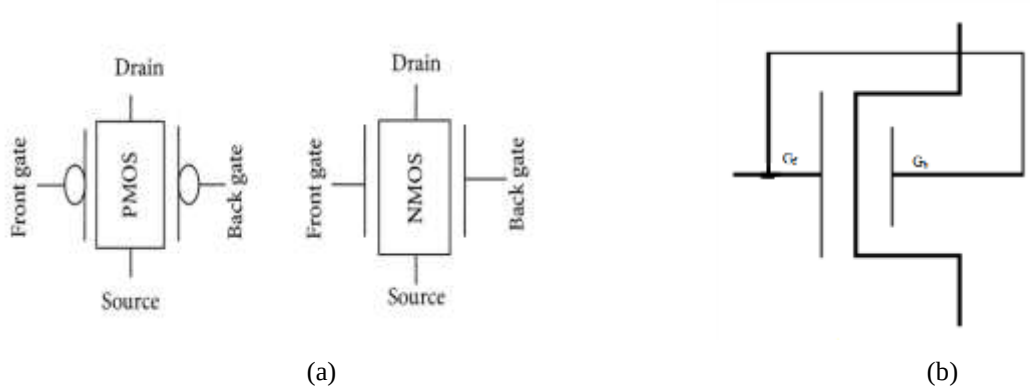
[2]. So, by using this model we can control the biasing one of the gate current flow, which makes it slower than the Short gate mode current but limited to logic transition as used as a logic switch. In Shorted Gate, The SG-mode NAND gate can be obtained directly by translating the CMOS NAND design to FinFETs, while retaining the same sizing it is a combination of two gates, best in replacement of bulk CMOS devices. It is a 3T device. [10] (fig. 2b)



(a) (b)

Figure 2: (a) FinFET & (b) SG

II. METHODOLOGY

The functioning of all decoders have been used in this paper is the same as considered it from the base circuit we use different technology and evaluate their parameter to get the best result. The basic symbol of Decoder is given above (figure 1) along with the truth table (table 1) So,in this section describe about all the method which are necessary to making 4 to 16 by using 2 to 4 decoder which are considering from previous research paper keeping in mind.[8]

Mixed logic structure contain transmission gate, pass transistor and base CMOS logic used in 2-4 line decoder to making 4-16 decoder FinFET. Pass transistor logic circuit are implemented with either Nmos/Pmos transistor. Pass transistor or parallel pairs of Nmos and Nmos known as transmission gates. In this logic an nmos or pmos transistor,or a cmos transmission gate can be used to transfer charge from one node of a circuit to another node, under the control of the FET gate voltage. Nmos transistor is an active high switching device which conducts and act as a closed switch when its gate voltage is high, HP refer to high potential in nmos. Pmos transitor is an active low switching device that conducts when its gate voltage is low, LP refer to low voltage in pmos. The bubble at the gate of the pmos transistor means that its gate must be at low voltage in order for it to turn on, the absence of a bubble at the gate of the nmos device means it conduct when its gate is at a high potential.

Transmission gate logic can efficiently implement AND/OR gate. It can be applied in line decoders. They are full swinging but not restoring for all input combination(figure 3).Dual value logic preserve the full swing operations of DPL with reduced transistor count. In complementary input are available the TGL/DVL gates require 3 transistor(figure 4).Decoders are high fan out circuits where few inverters can be used by multiple gates, thus using TGL and DVL can result to reduced transistor count.[13] In TGL gate input X controls the gate terminal of all 3 transistor, while input Y propagates to the output node through the transmission gate. IN DVL gates, input X controls 2 transistor gate terminals, while input Y controls 1 gate terminal and propagates through a pass transistor to the output. we will refer to X and Y as the control signal and propagate signal of the gate. Therfore, when implementing the function (A B) or (A+B)function. It is more efficient to choose the inverted variable as control signal.[5]

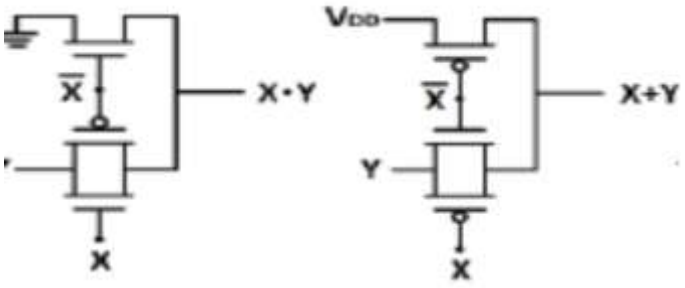


Figure 3:AND/OR gates using TGL

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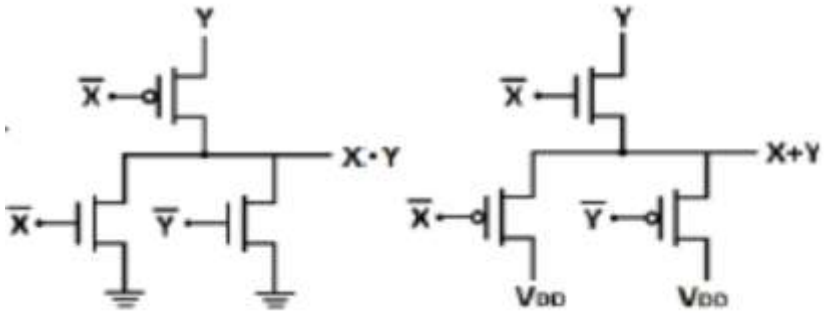

Figure 4: AND/OR gates using DVL

A. 14T 2-4 line Decoder

2-4 line decoder with either TGL or DVL gates would require a total 16 transistors(12 AND/OR gates 4 inverter).However, by mixing both AND gate types into the same topology and using proper signal arrangement, it possible to eliminate one of the two inverter, therefore reducing the total transistor count to 14. So by considering fig 3 & 4, show the use of the DVL which used in designing 14T. As all this already described in previous research paper, brief introduction is introduced about 14T.

Let us assume that out of the two input A and B, we aim to eliminate the B inverter from the circuit. The D_0 minterm (A' B') is implemented with DVL gate where A is used as the propagate signal. The D1 minterm (AB') is implemented with a TGL gate, where B is used as the propagate signal. The D2 minterm (A'B) is implemented with a DVL gate, where A is used as the propagate signal. Finally, The D3 minterm (AB) is implemented with a TGL gate, where B is used as propagated signal. makes B as propagate signal, and avert the use of complementary B, help to eliminate from the circuit and make it 14T. So, these are low power topologies with the disadvantage of scenario delay due to propagation signal utilization from D0. This is best choice for eliminating B inverter. 2-4 line decoder can be resulting by14-transistor topology (9 nMOS and 5 pMOS) and inverting mode of operation, we can consider (5nMOS & 9pMOS). [6]

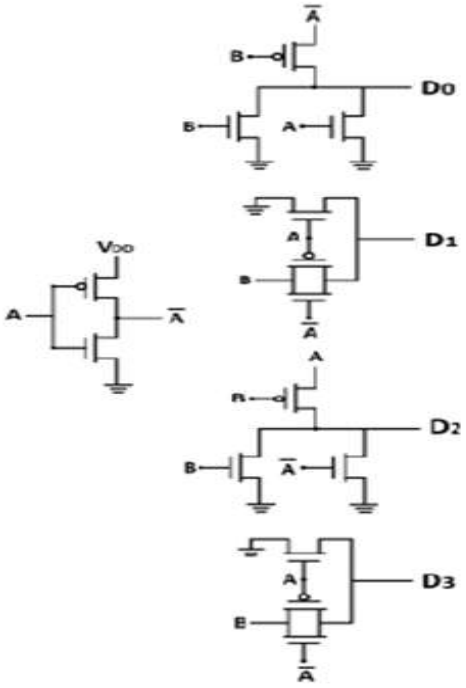

Figure 5: 14T 2-4-line decoders

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B. 15T 2-4-line decoder

As, It already described in previous research paper and by considering it for further improvement in designing 4-16 decoder, a brief description is given. So as we know the 14T or low-power topologies presented above have a drawback regarding worst case delay, which comes from the use of complementary A as the propagate signal in the case of D0. However, D0 can be efficiently implemented using static CMOS gates, without using complementary signals. Specifically, D0 can be implemented with a CMOS NOR gate and I3 with a CMOS NAND gate, adding one transistor to each topology. The 15T designs present a significant improvement in delay while only slightly increasing power dissipation and area. 2-4 line decoder can be resulting by 15-transistor topology (9 nMOS & 6 pMOS) and for inverting mode we can consider (6nMOS & 9pMOS).

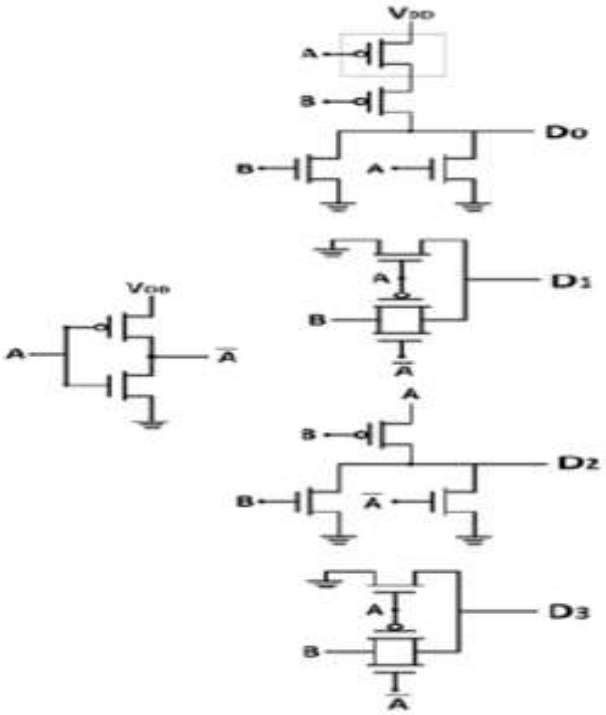

Figure 6: 15T 2-4-line decoders

C. **Multi-threshold CMOS (MTCMOS)**

MTCMOS is a technique in which it reduces the leakage current in stand by mode and attains high speed in active mode. It has transistors with multiple threshold voltages (Vt) in order to enhance delay or power. And High Vth transistor is used to isolate the lower Vt transistor from sleep and standby mode. Now by using low Vth devices for those inverters makes latch faster and using High Vt devices as sleep transistors for the rest of the latch makes it energy efficient compared to a single V_t approach, where you will compromise on one or the other thing among power and delay. PMOS transistor used as header switches off the power supply in standby or sleep mode and NMOS transistor used as a footer switches working in sleep mode. Inserting the sleep transistors splits the chip's power network into permanent power network connected to the power supply and a virtual power network that drives the cells and can be turned off. Typically, high-Vt sleep transistors are used for power gating. In this technique high threshold voltage transistor are used to isolate the low threshold voltage transistor from supply and ground during standby mode. However by including extra transistor, MTCMOS circuit faces performance penalty compared to CMOS circuits, if the transistor are not sized properly. The high threshold voltage transistor are turned off during standby (sleep mode) this result very low sub threshold passes from Vcc to ground MTCMOS includes high Vt transistor to gate power and ground of a low Vt logic blocks as shown in figure 7.when the high Vt transistor are off resulting in a very low sub threshold leakage current. When the high Vt transistor are turned on, low Vt are connected to virtual ground and Vdd.[11]

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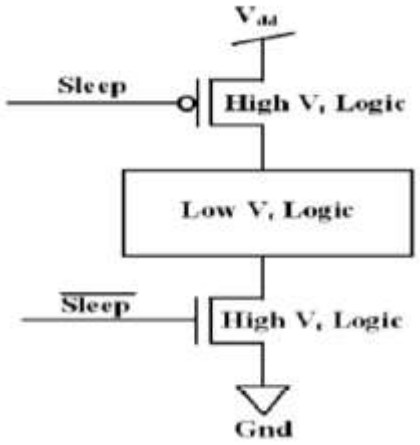

Figure 7: Basic MTCMOS technique

III. PROPOSED SYSTEM

Integration in 4-16 Line Decoder

In 4 to 16 decoders with mixed logic, 14 T and 15T configurations are used with NAND gate for inverting type decoders. 4–16-line decoder produces the 16 minterms D_0–D_{15} of 4 input factors A, B, C, and D, and an altering 4–16-line decoder creates the reciprocal minterms I_0–I_{15}. Such circuits can be executed utilizing a predecoding strategy.

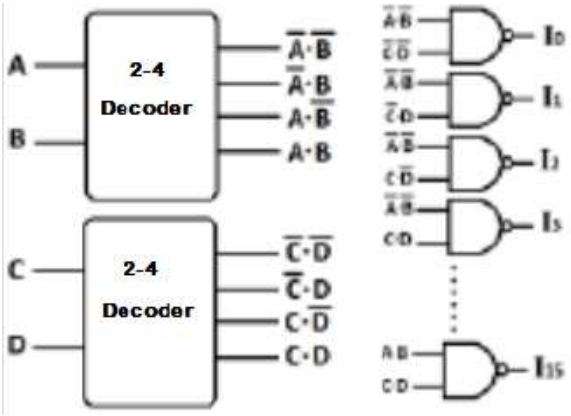

Figure 8: 4-16 decoder logical block diagram

Realization of figure 8 is a logic diagram of 2 to 4 decoder into 4 to 16 decoder in inverting mode. This requires two 14 Transistor (2*14), two 15 Transistor (2*15) and four transistor in 16 NAND gates (16*4) with mixed logic. The 14T topologies have a total of 92 transistors, while the 15T ones have 94 in mosfet based 4 to 16 decoder, 14T and 15T topologies have same numbers of transistors in FinFET based 4 to 16 decoder but by using 4 to 16 decoder 15T FinFET decoder we using MTCMOS technique in ground terminal so that we have total transistors 95. Although the numbers of transistor are same and we try to optimize on the basis of parameter delay, power, PDP, EDP. We use 4 to 16 decoder with mixed logic with NAND gate for simulation with 14T & 15T configuration. And we use 15T as proposed Circuit based on 4-16 decoder..
The circuit of the MOS decoder has been replaced by FinFET, we replaced 2 to 4 decoder by 4 to 16 by joining them as we know the basic of desiginng of decoder from 2 to 4 to 4 to 16 And then use a MTCMOS technique with 15T FinFET after that we can see that improvements and compare the all parameter.

By keeping the base logical circuit in mind fig. 8, all circuit implemented using 2-4 decoder.

We first made a 4 to 16 decoder with 14T MOS and 15T MOS after that, make a 4 to 16 decoder with 14T FinFET and 15T FinFET and then comparing the parameter like power, delay, Energy delay product, Power delay product by introducing MTCMOS in channel length of 22nm technology in FinFET.

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By using Hspice simulation software, we include model file 22nm technology, where all supply voltage are simulated at 1V and ground to 0V. In circuit topology we defined input voltage and output voltage on the basis of 15 decoder. In FinFET all substrate will be we give a pulse as input. In FinFet 15 based 4 to 16 decoder include pmos and nmos T_{Fin} thick, H_{Fin}, L, N_{Fin}, NRS and NRD are for activate region for source and drain. In proposed 15T finfet added a new transistor in ground path in replacement of ground 0, so all main circuit are changes to ground 0 to new transistor and give a new a signal also. we give a pulse in between new signal and new transistor which activate the sleep mode by this changes with respect to ground are all changed in the ground. then analysis transient of circuit. we measure circuit analysis by using transient analysis(measure value as a function of time t=1n to t=500n) then measure average power and delay by measure command (used to measure rise and fall time delay) voltage V(2) to voltage V(31). For getting the various parameter like PDP, EDP can be calculated by simple formulation which is describe next.

As we know that PDP is the Power delay product which is the combination of calculated power & estimated delay. And another factor is the EDP stand for Energy power delay which is the combination of PDP & delay. So these factor are very useful in comparing the losses or improvement in design by using different mode of operation or technology.

Schematics design

For schematic designing, LTSpice tool is used for designing the circuit. 4 to 16 decoder based on FinFET 22nm using SG-mode NAND gate. In short gate (SG) FinFETs the two gates (front gate-back gate) are connected together, leading to three terminal device. this can serve as a direct replacement for the conventional bulk CMOS device. Figure 9, you can see that NAND gate will be realize by using 4 transistor as FinFET in 22nm (nano technology) using Short gate mode as shown in schematic, here we can see in term PV_{gf}, PV_{gb}, NV_{gf}, NV_{gb} , PV_d, NV_d , PV_s and NV_s in P and N type, in this figure we can see that the front gate is connected to back gate which leads the device in 3 terminal and V_d is the drain voltage where as V_s is the voltage source. P type is Pull up and N type is Pull down network.

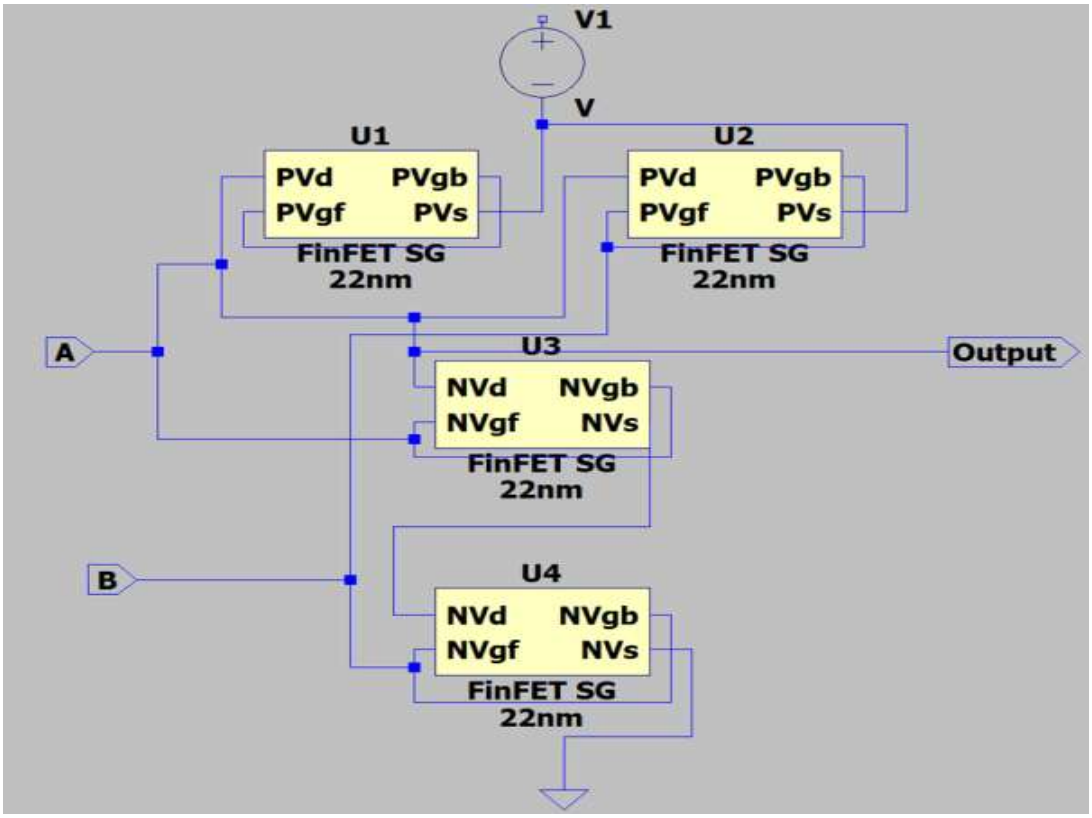

Figure 9: FinFET based NAND Gate 22nm

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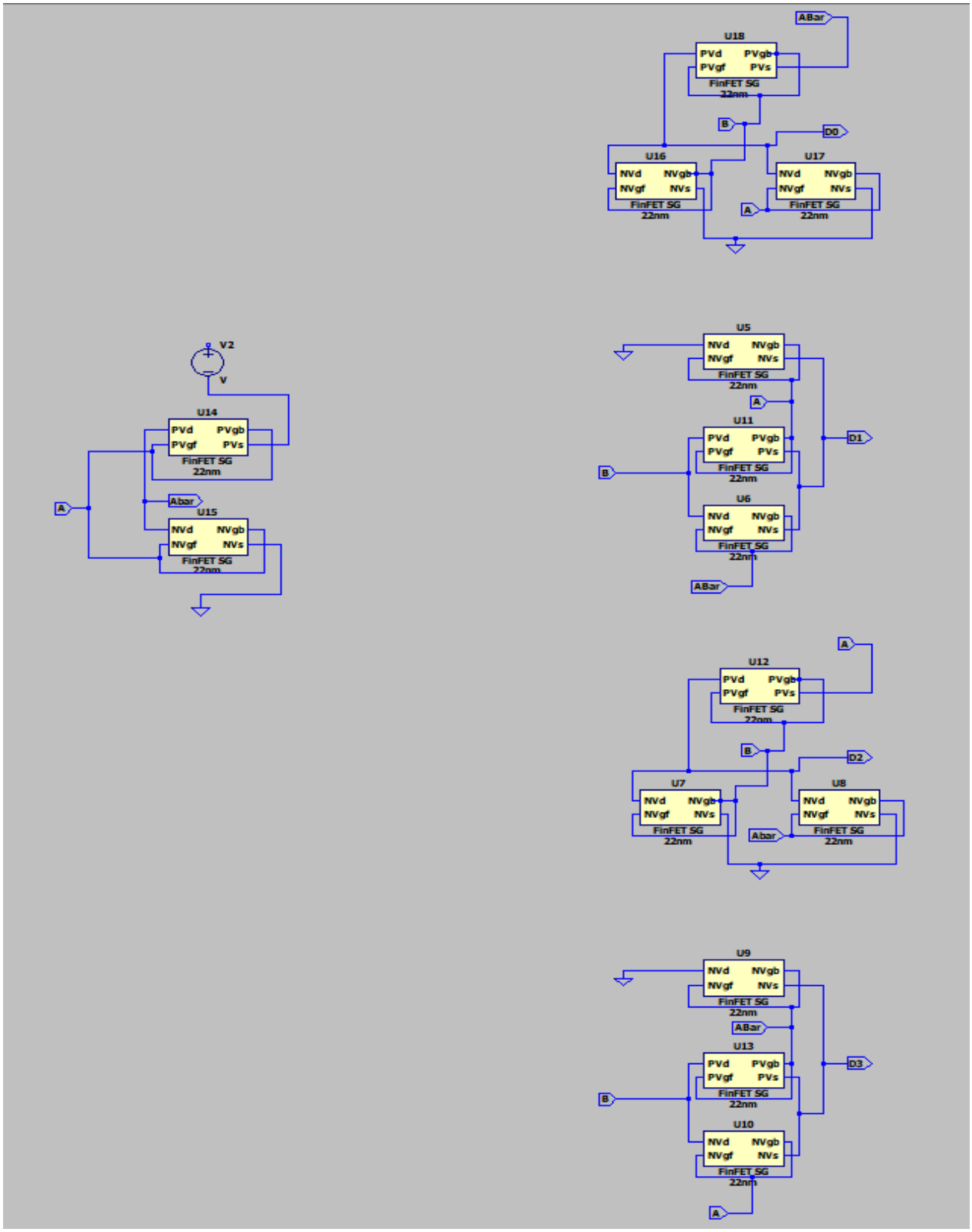

Figure 10: Schematic of 2 to 4 decoder using 14T FinFET

The schematic of 2 to 4 decoder using 14T FinFET as shown in figure 10.

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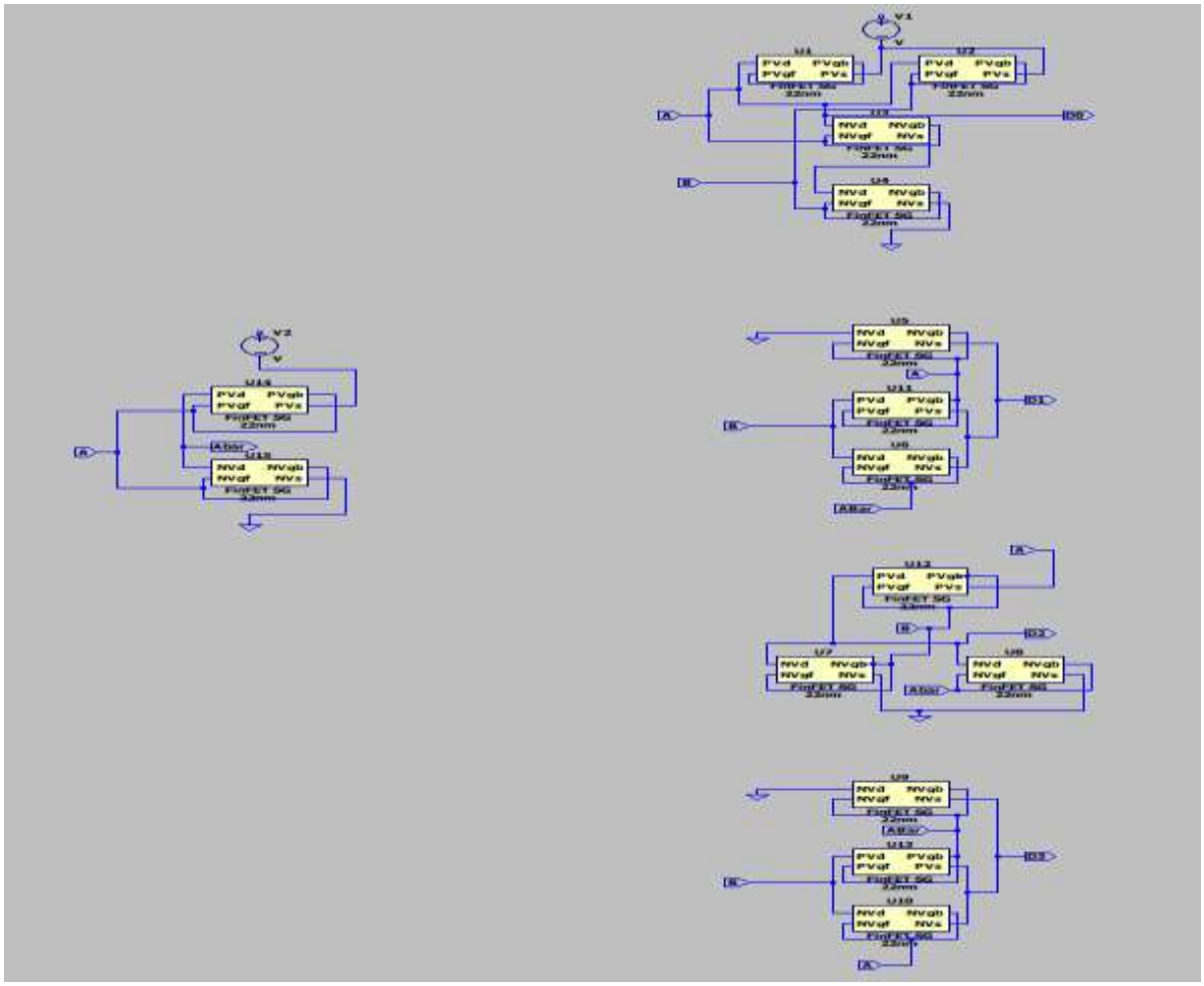

Figure 11:Schematic of 2 to 4 decoder using 15T FinFET

2 to 4 decoder is realize by the schematics of 2 to 4 decoder using 15T FinFET as shown in figure 11.

Figure 10 and 11, In schematics, you can see the 2 to 4 decoder based on FinFET, as we know the actual realization of 4 to 16 decoder here is little tricky as lots of transistor is includes which is more than 100, and showing each transistor here is difficult so by keeping it mind, taking basic building block of 2 to 4 decoder we design and compare the performance of 4 to 16 on using Hspice simulation software.

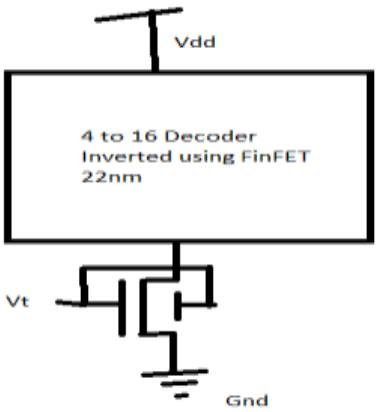

Figure 12: FinFET based 15T decoder logic 22nm with MTCMOS Signal (Proposed)

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In figure 12, the final proposed circuit topology based on FinFET based MTCMOS Decoder on 4 to 16-bit configuration is presented. As we already discussed MTCMOS in section II(C) in figure 7, they're working and how it useful in maintaining leakage current, which helps in lower power consumption.
So here, the Vt signal varies the threshold of the circuit. Thereby, giving a chance to improve all the parameters under consideration from the ground leakage path. we add a new transistor to the ground terminal of 15T in N-type Fin-FET called MTCMOS technique, we give a new pulse which will implement sleep and active mode and with respect to ground. We can see the Sleep wave in Output Waveform, which is described in the next section(fig.14)

IV. RESULTS

The simulation results are shown in this section table 2 presented in tabular form. The proposed FinFET based 4 to 16 decoder 22nm technology is performing better in power consumption, PDP, and EDP in all cases. Delay is almost the same acceptable in all cases.

Table 2: Proposed work for 4 to 16 decoder using MTCMOS based outputs

22nm	Decoder 4 to 16 with 14T MOS	Decoder 4 to 16 with 14T FinFET	Decoder 4 to 16 with 15T MOS	Decoder 4 to 16 with 15T FinFET	Proposed 4 to 16 with 15T MTCMOS
Power Consumption (watt)	1.13E-06	3.55E-08	1.16E-06	3.81E-08	2.67E-08
Delay(sec)	7.83E-08	7.81E-08	7.83E-08	7.81E-08	7.83E-08
PDP(joule)	8.82E-14	2.77E-15	9.11E-14	2.98E-15	2.09E-15
EDP(joulesec)	6.91E-21	2.17E-22	7.13E-21	2.33E-22	1.64E-22

In table 2, we can see that the FinFET comparison with MOS. Decoder. 4 to 16 with 14T FinFET value is 3.55E-08 which is better than decoder 4 to 16 with 14T MOS value 1.13E-06,Decoder 4 to 16 with 15T FinFET value is 3.81E-08 which is better than 15T MOS value 1.16E-06 in power consumption,15T FinFET MTCMOS value is 2.67E-08 which is gain by the changes in 15T FinFET.In delay 4 to 16 decoder with 14T MOS value is 7.83E as compared to 14T FinFET decoder value is 7.81E.whereas,the 4 to 16 decoder with 15T MOS value is 7.83E and decoder 4 to16 with 15T FinFET value is7.81E and 15T MTCMOS value is 7.83E almost change. In PDP decoder 14T FinFET and MOS value is 2.17E-15 and 8.82E-14. In PDP decoder 15T FinFET and MOS value is 2.98E-15 & 9.11E-14,15T MTCMOS value is 2.09E-15.EDP value of 14T MOS & FinFET is 6.91E-21 & 2.17E-22,15T MOS & FinFET value is 7.13E-21 &2.33E-22 and 15T MTCMOS value is 1.64E-22.

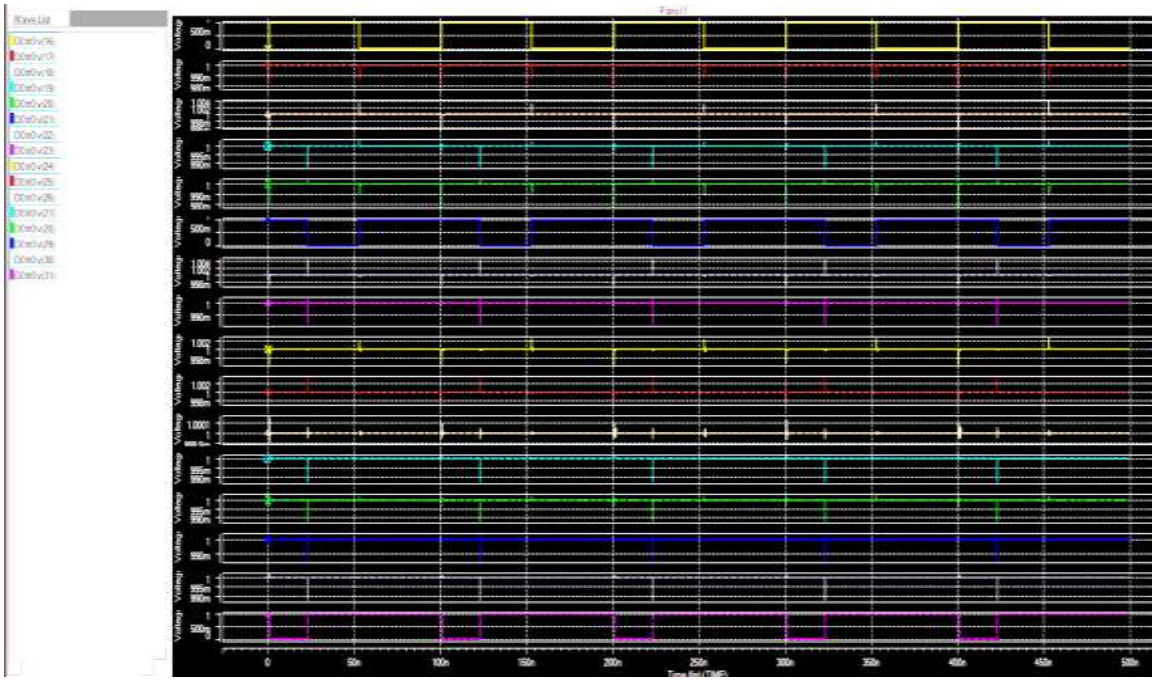

Figure 13: Waveform for Decoder

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Figure 13 show output waveform of 4 to 16 with 14T Decoder, follow waveform according to 4 to 16 decoder. the pulse form causes the voltage to start at V(2) and stay there for T_d 1 seconds. Then, the voltage goes linearly from to input voltage V(2),V(3),V(10),V(11).The voltage goes linearly from V2 back to V1 during the next Tf seconds. The voltage V1(0) and V2(1) in volt,the pulse time goes to Td(0)in sec,Tr(2n)in sec,Tf(2n),in sec, Pw(20n)in sec, Period(100n)in sec V(2),V(10) pw are same and V(11), V(3) pw are same and then the cycle is repeated like this. As we using NAND inverter , we can see the output at the last waveform as '0'.

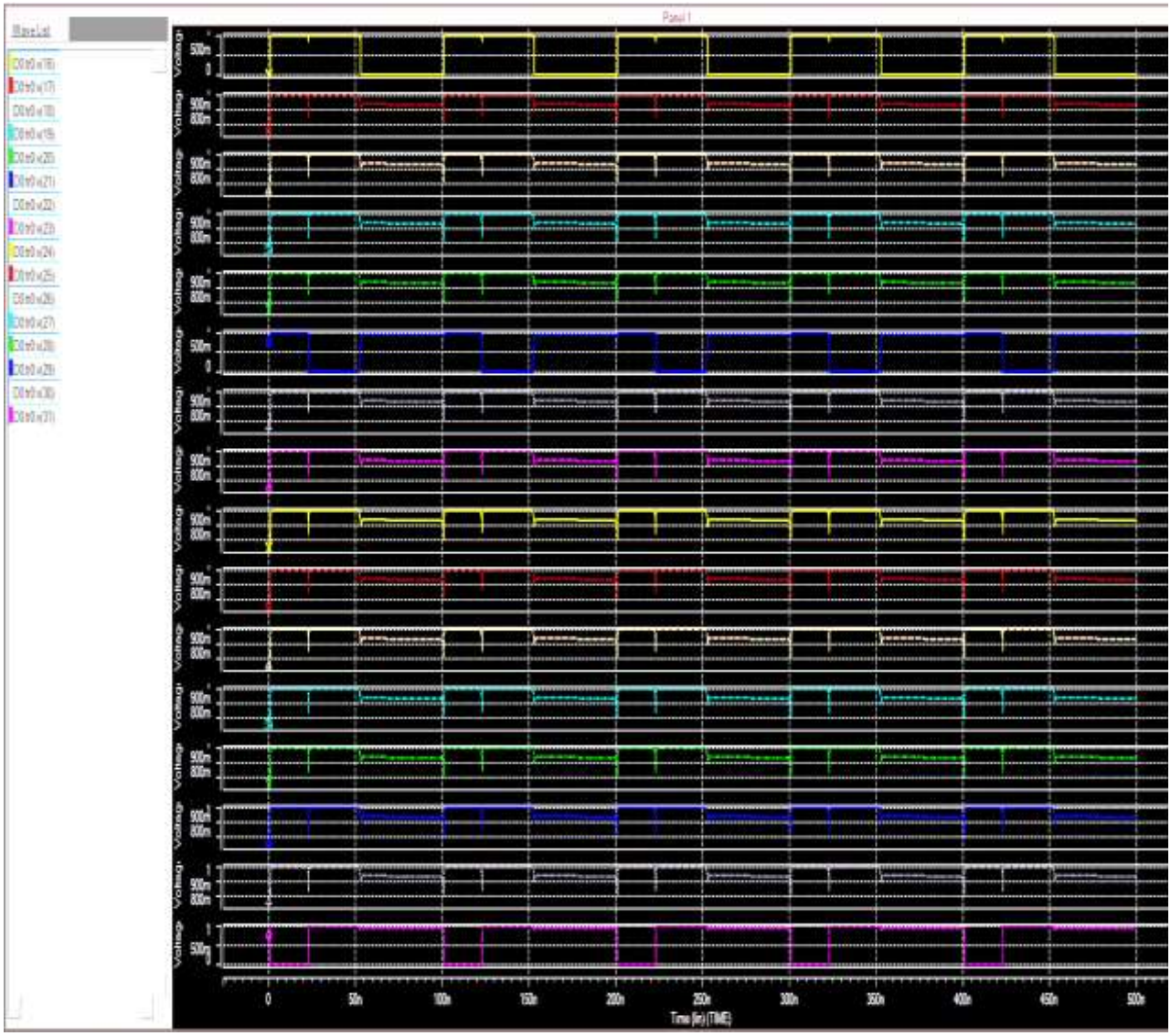

Figure 14: Waveform for Decoder with Vt threshold using MTCMOS (Proposed)

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Figure 14 shows the waveform of the proposed Decoder 4 to 16 with a 15T MTCMOS decoder, follow waveform according to 4 to 16 decoder.The pulse form causes the voltage to start at V(2) and stay there for Td1 seconds. Then, the voltage goes linearly from to input voltage V (2), V (3), V (10), V(11), and Vt V(31) for Pw seconds. The voltage goes linearly from V2 back to V1 during the next Tf seconds. The voltage V1(0) and V2(1) in volt, the pulse time goes to Td(0)in sec,Tr(2n)in sec,Tf(2n),in sec, Pw(20n)in sec, Period(100n)in sec V(2),V(10) Pw are same and V(11), V(3) are same and then the cycle is repeated like this.we give new pulse in Vt The voltage V1(0) and V2(1) in volt, the pulse time goes to Td(0)in sec, Tr(2)in sec, Tf(2n),in sec, Pw(50n)in sec, Period(100n)in sec and then the cycle is repeated like this. As we using NAND inverter, we can see the output at the last waveform as '0'.

V. CONCLUSION

We got results from the simulation platform. where we find that power consumption is reduced by using FinFET as compare to MOSFET, which makes it a promising substitute for MOSFET beyond 22nm technology, due to short channel effects. We can compare the high speed and low PDP, and Low EDP by the % value that is 42% improvement in power, 0.02 variation in delay, 42.5% 42.0% respectively improvement in PDP and EDP. So, by the controlling of leakage current in ground path terminal, our performance is better high.

VI. REFERENCES

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