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DESIGN OF CARRY SAVE ADDER WITH LOW POWER USING MODIFIED GATE DIFFUSION INPUT TECHNIQUE

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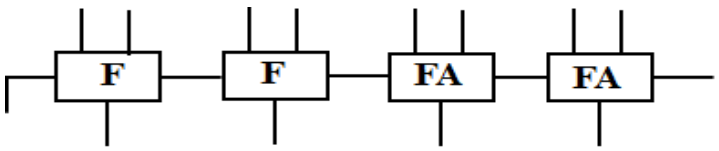
ABSTRACT:

It's a pretty digital adder, used to think in binary with little vogue in personal computer all three or more n-bit numbers. As a consequence of the inputs, it varies from entirely different digital adders because this it generates two numbers of constant lengths, one that can be a sequence of partial total bits and another that can be a sequence of carrying bits. A CSA tree consists of several complete block adder operators and one full adder at each tree level. The CSA process custom transfer associate in nursing discretionary differs from operands that display Using 3 1-bit binary numbers A, B and C, under which addition of operands would be specific using CSA and without using CSA. Carry Save Adder is a multi-quantity high speed adder that is used in many applications. Implementing CSA victimization CMOS can have a influence on power dissipation, delay in dissemination, and count of semiconductors. This paper accustoms with low-power and high-speed CSA design using the "Modified Gate Diffusion Input " technique in order to reduce transistor victimization. The "Gate Diffusion Input (GDI) methodology" follows this method. Examination with GDI technique, dissipation of power, delay of propagation and square count of semiconductors test several system side MGDI technique.

KEYWORDS: Carry Save Adder (CSA) , Low power dissipation, MGDI, GDI, High Speed

I. INTRODUCTION

In any automated device, adders play a huge role in arithmetic and computer circuits that can be used in the application of signaling methodologies. For any central method unit of a conveyable pc, arithmetic functions play an enormous role which therefore makes the researchers draw for tons as they reach to be used in many applications. And other additional elements such as CLA adder, carry skip adder, RCA etc. CSA is a low-cost, high-speed adder with less dissipation of cost and less latency compared to entirely different adders. Among advanced adders the RCA is the most commonly used primary adder. Within RCA's architecture, uses a one-bit cascaded complete Adders row to execute 2 added operands. Additionally, this row of complete adders can be organized as a way to scale back 3 binary numbers into 2 multi-operand binary numbers (three or additional operands), with a minor change to the present mogue. This method is used in CSA and connects RCA to its carriages that are processed instead of propagated in nursing. So CSA operator is usually referred to as counter (3:2). The block diagrams shown in Illustration 1(a) and Fig.1(b) for the RCA and CSA units respectively.



Fi g.1(a): Sample RCA block diagram

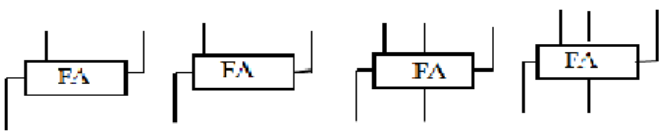


Fig.1(b): Sample CSA block diagram

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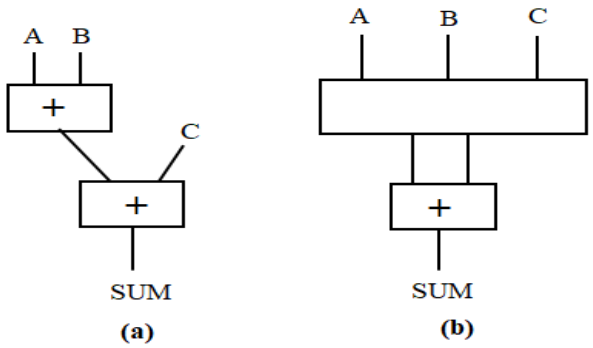
This paper outlines CSA's design process and operation, along with little reference to the MGDI technique. Later it offers 4-bit architecture through the MGDI technique of exploitation. Ultimately, the area unit results compared to power dissipation, spread delay and semiconductor unit count with CMOS communication and GDI technology.

II. INITIATION TO CARRY SAVE ADDER (CSA)

The CSA tree is composed of complete adder at each point and one bit full adder at the tree's inspiration. The CSA measurement unit accustomed to build over associate in nursing discretionary varies from operands within the addition technique 2 Add operandi, If the adders determine the final word total at the inspiration of the CSA tree from operands within the addition technique to generate 2 adding operands. Fig.2 indicates the Using 3 1-bit binary numbers A, B and C, severally applied but not the CSA operator and the CSA operator



a) Without operation by CSA b) Operating with CSA

Fig.2: Summation process

As mentioned above, the 1-bit multi-operand addition approach was extended to include the introduction of n-bit multi-operand in nursing by cascading the CSA tree which is associated in N-bit CSA consisting of n disjoint complete Adders operating in parallel. Each block of units has the data in nth bit and produces 2 outputs i.e. Sum and carry where the total sum is represented as S and the carry is represented as C. When the addition bits expand, additional successive rates of CSA operators are introduced. The number (S) and carry(C) outputs are obtained from the previous stage of operator Carry Save Adder. The recent sum is given as an input to the next stage of CSA operator in conjunction with another input quantity while the carry is stored in place of propagation. The carry will only propagate in the last propagation process. Accordingly, compared with RCA propagation delay with n complete adders, save Adder bears the same delay in propagation as in 1 unit only and is constant for any value of n.

Carry Save Adder has four binary 4-bit numbers A, B, C, and D, in which C is given as the initial input. Carry Save Adder's upper two levels are associated as (3:2) 4-operand 4-bit CSA counters, while the lower level is associated with 4-operand 4-bit RCA. Can also use the CLA Adder as a fast adder, rather than using Carry Adder Ripple. Each CSA operator takes three bits of input which are of the same meaning and generates sum and carries the same meaning in each point.

The Carry Save Adder can be implemented further by extending K operands for addition. Here one level of CPA and (k-2) of CSA is necessary for the addition. The time needed to get the estimate is

$$T = (k-2).\ TCSA + TCPA \quad (1)$$

Equation (1) includes the time required to get the CSA K-bit implemented. TCSA and TCPA represent the execution times for a CSA and CPA stage respectively.

III. GATE DIFFUSION INPUT(GDI) TECHIQUE

GDI is technique of low power. The basic GDI cell consists of a pair of transistors alone, such as NMOS and PMOS transistors. GDI approach allows maximum variety of sophisticated logic functions to be implemented. It's applicable for logic implementation of less vary of transistors compared to the CMOS logic.

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The GDI technique uses a basic GDI cell that look just like the basic CMOS inverter and remains one in every of the standard CMOS invertor, and has some exceptional variations that unit listed below.

The GDI technique is technique of low power and it's the name itself that one of the inputs is supplied directly to one of the NMOS and PMOS transistor gates. The elemental GDI cell consists of a pair of transistors such as the transistors NMOS and PMOS.

GDI logic vogue implementation allows for broad-based functions with a pair of transistors. This technique embraces the kind of high-speed and low-power circuits that will minimize the transistor parameters varying from techniques CMOS and current Pass Transistor Logic (PTL).

The primary GDI cell consists of 3 inputs: G (common input to NMOS and PMOS gate), P (input PMOS to produce) and N (NMOS input to produce), while there are no three inputs in the CMOS converter circuit. Mass of each NMOS and PMOS area unit attached separately to N or P. Therefore each will be biased when separated from the CMOS converter. It should be noted that not all functions of the area unit come into operation in the normal CMOS technique in P-well, these are successfully implemented in Twin-well CMOS or SOI technologies.

The implementation of basic GDI cell permits the logic functions victimization of two transistors that may not come available with CMOS inverter.

Along with this GDI cell, the simple logic gates and universal gates are noted; the GDI logic vogue approach consumes less Si house than entirely different logic types, which can be seen from the particular established fact that the world may be a smaller number, The price of node capacities indicates a decrease and, the GDI gates are therefore running faster, meaning GDI logic vogue may also affect the economic style technique.

The fundamental GDI cell uses p-type and n-type transistors that use p-well, n-well or twin-well (Though CMOS transistors p-well and n-well can only be used for a limited range of logic circuit configurations), SOI transistors, SOS transistors, etc. in all probability area units. There is an incontrovertible fact that the excellence between the availability and drain of the semiconductor cannot be achieved by means of the GDI logic vogue, as long as any {transistor junction semiconductor electronic transistor semiconductor unit semiconductor unit}. The comparative voltages between the transistor diffusion node differ according to the input logic and the output voltages that differ from the normal complementary CMOS configuration while the availability or drain is coupled with the unremitting voltage.

In GDI technique N, P, G terminals area unit provided to power supply or are often grounded or sometimes applied with circuit-based input signals that effectively reduce transistor no. The GDI cell has 3 inputs:

1. G (Common feedback to the PMOS and NMOS destinies)
2. N (NMOS Source / drain input)
3. P (PMOS Source / Drain input)

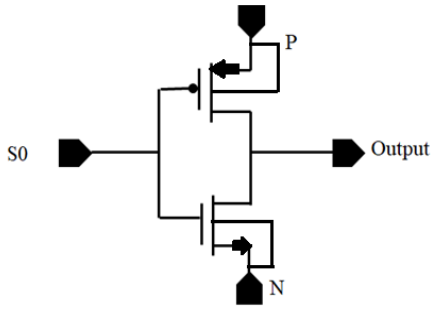

Fig.3: Basic GDI cell

Bulk of PMOS and NMOS area units attached separately to the 'P' or 'N' terminals.

However, GDI have some disadvantages i.e;

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- The most significant quality that GDI logic vogue faces is issue in fabrication customary CMOS methodology.
- Additional electronic equipment is required to offer inputs to the GDI based mostly circuits.
- The power consumption, propagation delay and transistors count square measure additional in GDI technique compared to MGDI technique.

Gate Diffusion Input technique is implemented due to improvements in addition to limitations. So, we prefer to implement MGDI technique because of this.

IV. MODIFIED GATE DIFFUSION INPUT TECHNIQUE (MGDI)

Modified Gate Diffusion Input (MGDI) may also be a new technique that replaces the vogue of the modern low power circuit. MGDI is obtained using the Gate Diffusion Input (GDI) method. The MGDI technique has become mainly familiar for trimming power dissipation capability, total propagation delay and summing up the digital circuits of semiconductor devices.

Nonetheless, among those variable units that have exploited the GDI technique, the MGDI technique is designed to address the GDI technique 's key required shortcomings such as weaknesses in manufacturing technique and additional equipment for supply of loads to circuits for the GDI building. By victimizing this technique, the combination logic gates such as OR gate, AND gate, inverter and multiplexer unit plot victimization for a pair of transistors, while four electronic junction transistor units used for OR & AND logics and the transistor count for multiplexers are fourteen CMOS victimization vogue. The Modified-GDI technique could therefore also be a useful technique for chopping back the realm and, together, for less total dissipation of the circuit power.

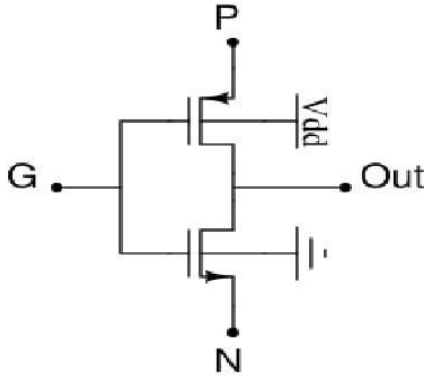

Fig.4:Primary MGDI cell.

N	SN	P	SP	G	Output	Function
0	0	1	1	A	A1	Inverter
A	0	0	1	B	AB	AND
A	0	B	1	A	A+B	OR
B^1	0	1	1	A	A1 B1	NAND
0	0	1	1	A+B	$(A+B)^1$	NOR
A^1	0	A	1	B	A^1B+AB^1	EX-OR
A	0	A	1	B	$AB+A^1B^1$	EX-NOR

Table1: Performance table of MGDI technique.

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Table 1, displays the input arrangement by the primary MGDI cell of the various parameters that unit achieved. For every Complementary Metal Oxide Semiconductor and MGDI technique, the inverter input arrangement is the same, and the facility dissipation will not be distinguished at intervals by either. The last remaining roles differ according to arrangement. The output of the basic MGDI logic cell once the input of the load is given and the generalized equation is given as

D= PG' + metric weight unit (2)

The primitive base of the MGDI cell is similar to that of the GDI cell consisting of four terminals G (common NMOS and PMOS transistor gate inputs), P (external PMOS transistor diffusion node), N (external NMOS transistor diffusion node), and Out (common transistor diffusion node). In modified primitive GDI cell body or PMOS substratum the supply voltage VDD is connected and the PMOS body is connected to the supply voltage field. Whereas in the GDI cell the PMOS body is connected to the drain, and the NMOS body is connected to supply it. This induces the GDI in modified GDI cell to constant

biasing of the body which in effect increases circuit soundness and its effects on loading. The unit area logic gates enforced in 130 nm CMOS technology and is compared to the existing logic of GDI and CMOS.

In order to produce tons of output, change the configurations like modifying to realize higher summation. Table 2,3,4 reflects the variations between the dissipation of electricity, the counting of semiconductor devices and the delay in propagation of various primitive gates. The logic gates are designed for the inverter to assume 2 inputs.

Primitive gates	**Power dissipation in nano watts**	
	CMOS	**MGDI**
Inverter	91.473	21.190
AND	9.29	$6.48X10^{-5}$
OR	59.19	$6.47X10^{-5}$
EX-OR	183.19	9.34
NAND	1.7896	77.27
NOR	152.55	77.276

Table2: Comparison of Power dissipation of different primitive gates in CMOS and MGDI techniques.

Logic gates	**Number of Transistors**	
	CMOS	**MGDI**
Inverter	2	2
AND	6	2
OR	6	2
EX-OR	12	4
NAND	4	4
NOR	4	4

Table3: Comparison of Number of Transistors of different Logic gates in CMOS and MGDI techniques.

Logic gates	**Propagation delay in nano seconds**	
	CMOS	**MGDI**
Inverter	20.8	19.25
AND	30.5	19.95
OR	29.69	18.08
EX-OR	102.5	29.15
NAND	20.57	16.49
NOR	40.97	19.0

Table4: Comparison of Delay of Propagation of different primitive gates in CMOS and MGDI techniques.

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From Table 4 it is stated that power dissipation in MGDI technique is significantly reduced compared with CMOS and GDI techniques. Hence, MGDI system is enlarged for highly complicated logic circuits where dissipation and delay of power are necessary in conjunction with fewer space.

V. REQUIREMENTS FOR USING MGDI TECHNIQUE TO DESIGN CSA

used as straight forward Ripple Carry Adder during the last point As previously mentioned, the CSA tree is composed of several complete blocks of adder operations and one full adder at each tree level. The generalized CSA diagram of Fig.4 displays n bit additions. It is confirmed that the carry propagate adder.

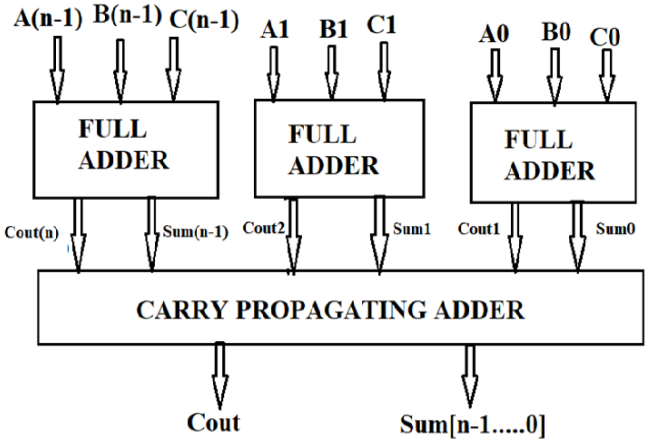

Fig.5: Basic Carry Save Adder block diagram by n-bit.

VI. 1-BIT FULL ADDER MODEL

Complete adder may be a combinational logic circuit that adds 3 binary digits. This can be a necessary building block for coming up with a VLSI system. Full adders are employed in sizable amount in arithmetic processors. It's a crucial building block in number circuits, dominantly influencing the speed of the latter. The fascinating characteristics of full adders are low rise and fall times, totally reconditioned logic levels at the output for such as load.

Although several analyzers have already plotted full CMOS 1-bit adders, this paper also reveals complete adder variations for the CMOS with 28 transistor numbers with full GDI adders.

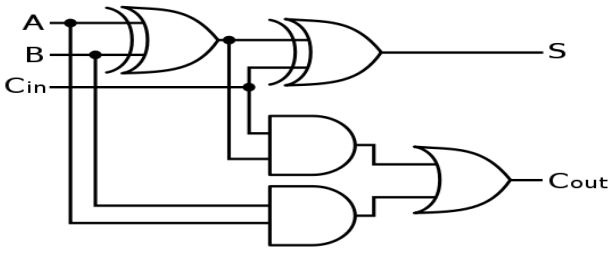

Fig.6: Logic diagram of Full Adder

The Complete Adder 1-bit is also built using MGDI technique. The equations of 1-bit Complete adder logic is shown respectively in equation (3) and equation (4).

$$Sum = A`BCin + AB`Cin + ABCin` + A`B`Cin` \quad (3)$$

$$Carry = AB + BCin + CinA \quad (4)$$

Full adder consists of 3 inputs that are Augends, number and Carry input. the 2 outputs are total and carry. It's clear that once the total output is one once either of inputs are one. Carry output is one once any of the 2 outputs are one or all of the inputs are one. Similarly, the logic expression for carry output as a total of product of expression by

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summation the input combos that the carry is adequate one. The total output corresponds to the logic EX-OR perform whereas the carry output corresponds to an AND performance. So, that full adder circuit is enforced mistreatment EX-OR, AND and OR gates.

Therefore, thanks to less power dissipation in NOR gate mistreatment MGDI technique the complete adder may been enforced mistreatment all NOR gates as shown below.

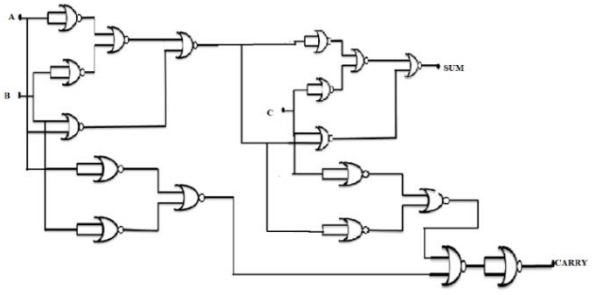

Fig.7: Circuit diagram of Full Adder using NOR gates in MGDI technique.

VII. DESIGNOF CSA 4-OPERAND 2-BIT

A 2-bit CSA can be implemented by exploiting half-dozen complete three-block adders within which 1st 2 blocks represents the CSA and thus the last block is the RCA.Within the addition system, the CSA operation is used to remodel the associate degree discretionary range of operands to provide 2 addition operands, once the addition is performed, another bit of data can be added for the Carry Save Adder tree which calculates the total addition cycle.

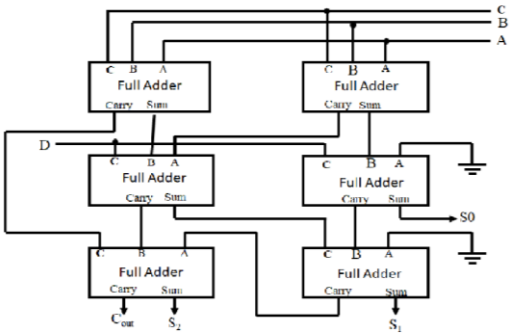

Fig.8: Block diagram of 4-operand 2-bit Carry Save Adder

Design technique	Total Power dissipation in nano watts	Transistor Count	Propagation delay in ns
CMOS	99.2	28	47.03
MGDI	0.0388	12	33

Table 5: Comparison of various parameters in CMOS and MGDI technique for a one-bit full adder.

It is shown from the above table that the MGDI technique provides less total power dissipation and delay in propagation including transistor count. So, due to reduction of the above parameters MGDI technique is employed in several advanced styles.

VIII. PROPOSED CARRY SAVE ADDER

Design of 4-operand 4-bit Carry Save Adder

Similarly a four-operand 4-bit carry save adder is intended exploitation twelve full adders in three blocks that during which within initial two blocks consists of eight full adders that's carry save adders and therefore the last

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block consists of 4 full adders which may be a carry look ahead adder, The carry look ahead adder can carry a cascading to the preceding state. The fig.9 below stands for the 4-operand 4-bit CSA.

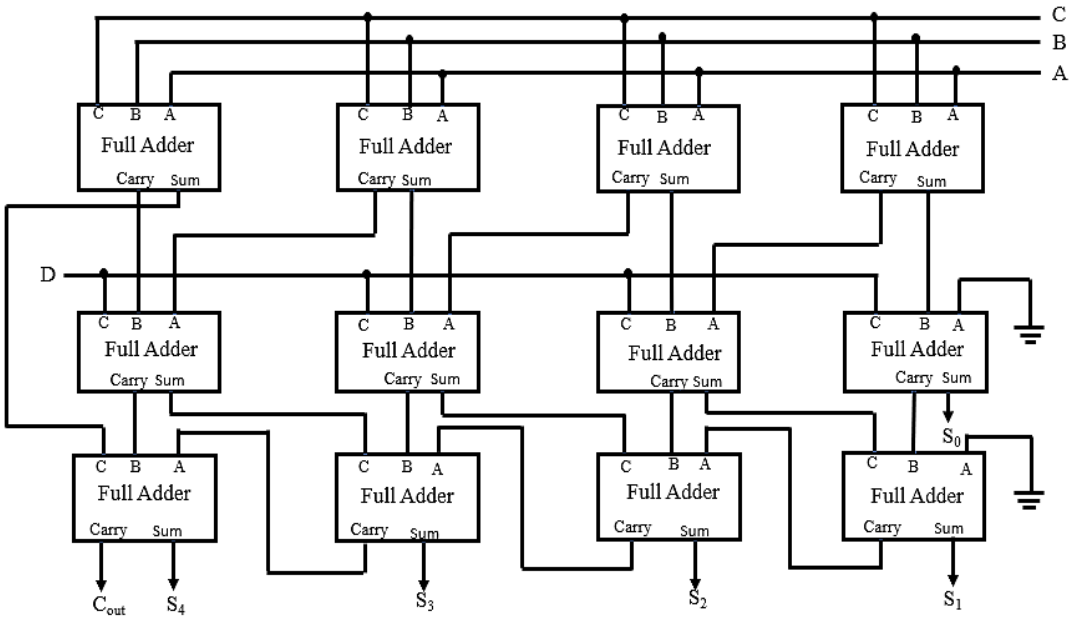

Fig.9: 4-operand 4-bit block diagram of carry save adder

Therefore, a 4-operand 4-bit CSA is enforced exploitation twelve FA's wherever A, B, C, D area unit four input operands and S0, S1, S2, S3, S4, Count area unit the outputs. the primary two rows represent the CSA and therefore the last block represents the carry propagation adder wherever the carry is propagated to the previous full adder whereas in CSA the carry isn't propagated instead the carry is one bit turned and at last added with the total. Below is that the truth table for 4-operand 4-bit CSA during which the provision voltage is given as 5v and therefore the patterns area unit given to inputs and therefore the corresponding outputs area unit determined.

IX. IMPLEMENTATIONOF 4-OPERAND 4-BIT CARRY SAVE ADDER

All the simulations are created by victimization MENTOR GRAPHICS code, Generic 130nm technology. The schematics are drawn by victimization PYXIS SCHEMATIC editor. The 4-operand 4- bit CSA is enforced by victimization FA's below CMOS and MGDI techniques. The simulation results are compared in transient analysis.

The below figure shows the 4-operand 4-bit carry save adder within which A, B, C, D are the input operands and S0, S1, S2, S3, S4, Cout are the outputs.

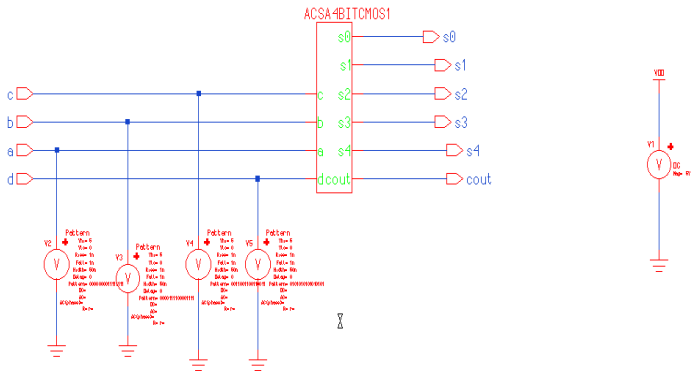

Fig.10: Simulation diagram for 4-operand 4-bit CSA in CMOS technique

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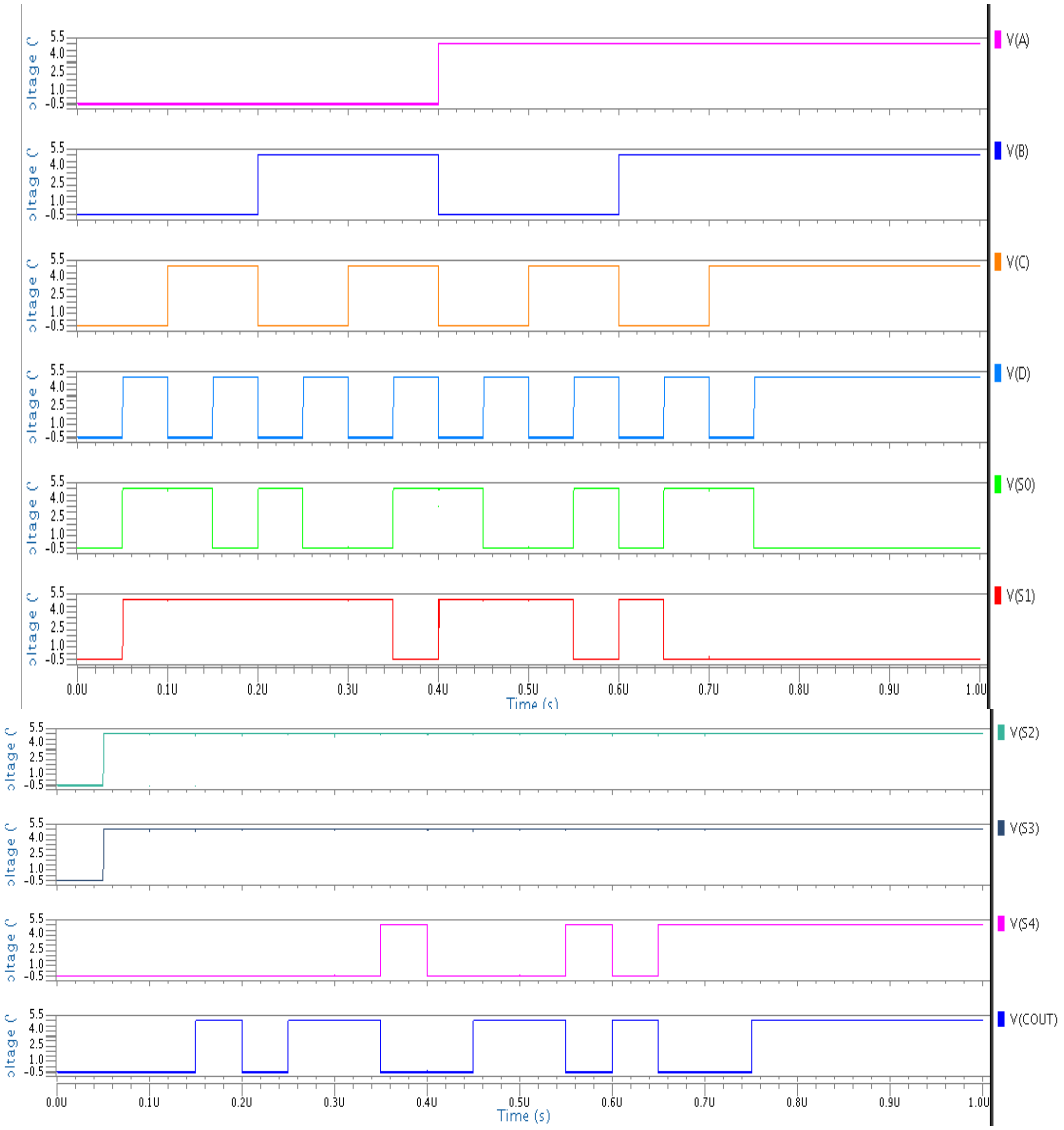

Fig.11: Output Waveforms for 4-operand 4-bit CSA in CMOS technique

Fig.12, Shows the simulation picture for the specified four operand and four-bit CSA, obtained from the full one adder configuration that has been tested for all the combinations, certain input and output combinations are as shown in Fig.13.

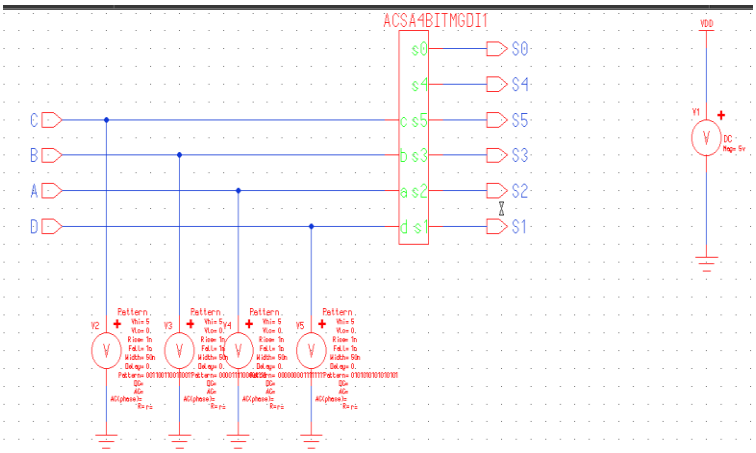

Fig.12: Simulation diagram for 4-operand 4-bit CSA in MGDI technique

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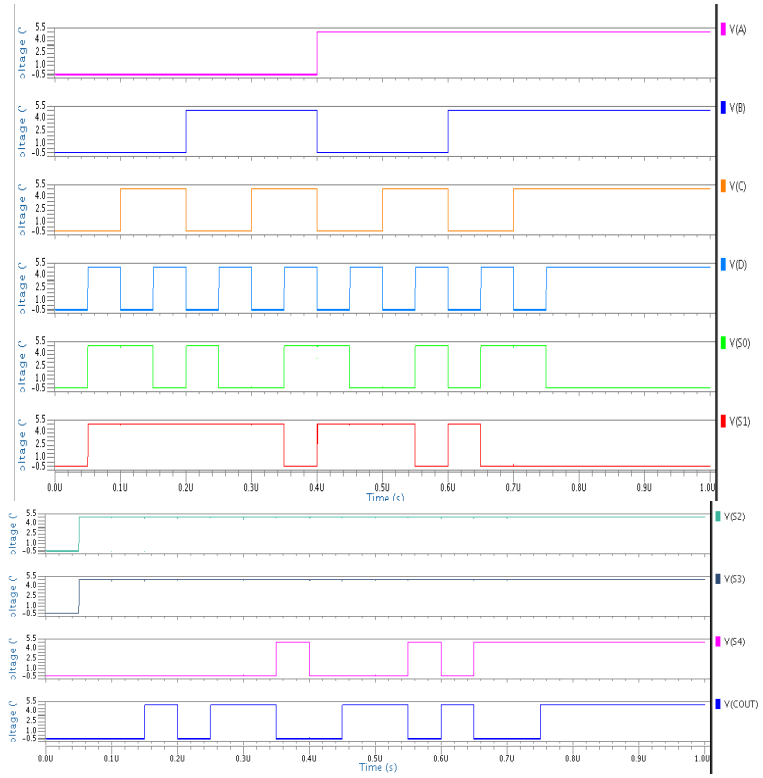

Fig.13: **Output Waveforms for 4-operand 4-bit CSA in MGDI technique**

CARRY SAVE ADDER	PROPAGATION DELAY		TOTAL POWER DISSIPATION	
	CMOS	MGDI	CMOS	MGDI
4-operand 2-bit carry save adder	568ns	49.9ns	10.34uw	6.93uw
4-operand 4-bit carry save adder	663ns	79.54ns	20.68uw	13.86uw

Table 6: **Comparison table for 4-Operand 2-bit and 4-Operand 4-bit CSA in CMOS and MGDI techniques**

X. CONCLUSION

High-speed and low-power applications are now supported in low power application. Low power applications is often the primary demand of advanced VLSI technology, that depends on provide and ground potentials. at first, we have a tendency to are studied the CMOS technique and ascertained that it's giant chip space and high-voltage consumption. to beat this method, we've suffered changed Gate Diffusion Input Technique (MGDI). we have a tendency to found that MGDI technique has several benefits than the Complementary Metal chemical compound Semiconductor (CMOS).

This piece of work verified that the MGDI technique was the best technique to promote less dissipation of power, a delay in propagation over the prevailing CMOS technique. This project is initially aimed at reducing the delay in propagation and the transistor count for logic gates. At the end of all the cases MGDI technique is discovered to be better than the other techniques. In 90 nm technology all results were compared with 5v supply voltage, it is additionally verified that one-bit full adder exploitation NOR gates are dissipating less power and fewer propagation delay with reduced number of transistors. Therefore, among many adders the most powerful adder is referred as CSA, and it can be designed in two bit, four bits and so on as a power of two. Propagation delay is measured in terms of time taken by the input and output resources. Thus, the adder can create the highest delay as

for the dissipation of power, power consumption, delay in distribution and the circuit counting transistors. MGDI technique therefore exhibits less power, delay and reduced chip space.

XI. FUTURE SCOPE

In future, 4-bit Carry Save Adder victimization numerous techniques may be enforced to optimized less power dissipation. Further, CSA may be used for planning a number. we can implement multipliers by victimization MGDI technique to perform multiplication operation and these multipliers may be perform higher than CMOS multipliers. Further, this superior CSA may be enforced in sensible mobile phones and calculated devices. The proposed style can be improved by replacing each FA stage with adder so that the speed can be increased by nearly 60 percent. Nevertheless, all of this is also opportunity at the expense of any space & power exchange. If all 3 CSA phases are scheduled with CLA Adder then the propagation delay will be enormous in calculation.

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