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READOUT INTEGRATED CIRCUIT WITH ADDED CLOCK GATING FEATURES TO ACHIEVE MINIMUM-POWER AND GREAT SENSITIVITY

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ABSTRACT: This paper addresses the ReadOut Integrated Circuit (ROIC) with added features of low power and high sensitivity focal plane array. The capacitor-reset block employing clock signals adopts a double-edge-triggered flip-flop. For low supply voltage operation three single event upsets flip flop topologies are used. This flip-flop topologies shows the ability of achieving maximum SEU cross-section. In addition, an asynchronous clock-gating technique is employed to control clock-signal usage in accordance with the input signal, thereby reducing the power consumption within two-dimensional arrays. Low-power, high-sensitivity ROIC has been realized with a 0.18-μm 1-poly 6-metal CMOS process. This ROIC can be reduced power consumption to approximately 2% of than conventional ROICs.

KEYWORDS: Clock gating, sensitivity, Read out integrated circuits, single event upsets, CMOS.

I. INTRODUCTION

Mid-wavelength infrared (MWIR) focal-plane arrays employed in defense applications, such as missile system, must meet the requirements of high dynamic range, low power consumption and a high sensitivity. A high dynamic-range readout integrated circuit (ROIC) characterized by an asynchronous self-controlled two-gain-mode operation and multiple reset control was recently proposed in accordance with the input signal for each pixel was recently proposed. To facilitate high-dynamic-range operation in this ROIC, a 10-MHz clock signal was used to generate a 100-ns pulse signal that resets the integration capacitor. This pulse width, albeit small, may cause an error to exist within the final output signal. This implies that the occurrence of an integration time difference of 100 ns between similar input signals may cause differences to exist within the output signal. Meanwhile, in conventional high-dynamic-range ROICs,a clock signal is provided as input to all pixels regardless of the input signal. However, when the input-signal current is low, the use of the clock signal becomes redundant, thereby results in excessive, unwanted power consumption of ROICs. In this study, the use of a capacitor-reset block has been employed with a double edge-triggered (DET) flip-flop instead of a single-edge-triggered (SET). One is proposed to facilitate the reduction of errors within the final output signal. In addition, the use of an asynchronous clock gating technique in combination with ROIC internal signals is proposed to reduce the power consumption within 128 × 128 arrays. The utility of the proposed circuit was demonstrated through the post-layout simulations. Low power electronics have been one of the main areas in commercial complimentary metal-oxide semiconductor (CMOS) electronics in last two decades. However, the interest for low power exists in high reliability application areas such as space applications. The obvious reason for low power electronics being attractive in space applications is the limited power budget in spacecraft, for example when the power supply is dependent on solar cells.

In sequential CMOS circuits, SEU mitigation techniques often rely on supply voltages being as high as possible in order to attain the best possible SEU tolerance. When the supply voltages reduces then the internal

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nodes become more susceptible. On another way, the power consumption of an integrated circuit (IC) is reduced by reducing the supply voltage. Power consumption have been saved up to several orders of magnitude. One more advantageous point of low supply voltage operation is that its Total Ionizing Dose (TID) induced leakage decreases. This low TID induced leakage is important for realizing both low power and reliable ICs. This work is the first to investigate the general effects of temporal and spatial hardening techniques on the SEU. This is done as a function of a wide supply voltage range from 180 mV to 1 V. Obtained results show that the temporal hardening has higher impact on the SEU sensitivity of the studied DFFs at supply voltages above 500 mV. But spatial hardening has maximum effect on the SEU sensitivity when supply voltages below 500 mV. DFFs used in this work is operated at a supply voltage of 500 mV without experiencing any SEUs. Even 72% more energy efficiency attained than a Dual Interlocked Storage Cell (DICE) DFF at 1 V supply voltage. The DFFs are compared in terms of area, clk-to-Q delay, setup time, energy per transition and maximum frequency. Besides, a DICE-based DFF is also included to serve as a reference DFF. To improve the SET tolerance and power consumption of the capacitor reset block used in the ROIC, Dual feedback edge trigger DFF is designed by integrating dual feedback logic with double edge trigger logic. Compared to other flip-flops, DFET offers advantages in terms of speed, power and error.

II. PROPOSED SYSTEM

Existing system failed in following points: i) The existing system is to consume more power and to increase the circuit complexity level in testing process. ii) Low reliability level in testing. iii) Need more time for read/write operation process. In this ROIC, the capacitor-reset block employing clock signals adopts a double-Feedback-edge triggered flip-flop is used to reduce errors within the final output signals. In addition, an asynchronous clock- gating technique is employed to control clock-signal usage in accordance with the input signal, thereby reducing the power consumption within two-dimensional arrays. The work has been realized with CMOS process having a 0.18-µm 1-poly 6-metal. It has been found that in low input-signal current, the power consumption of the proposed ROIC can be reduced to approximately 2% than conventional ROICs.

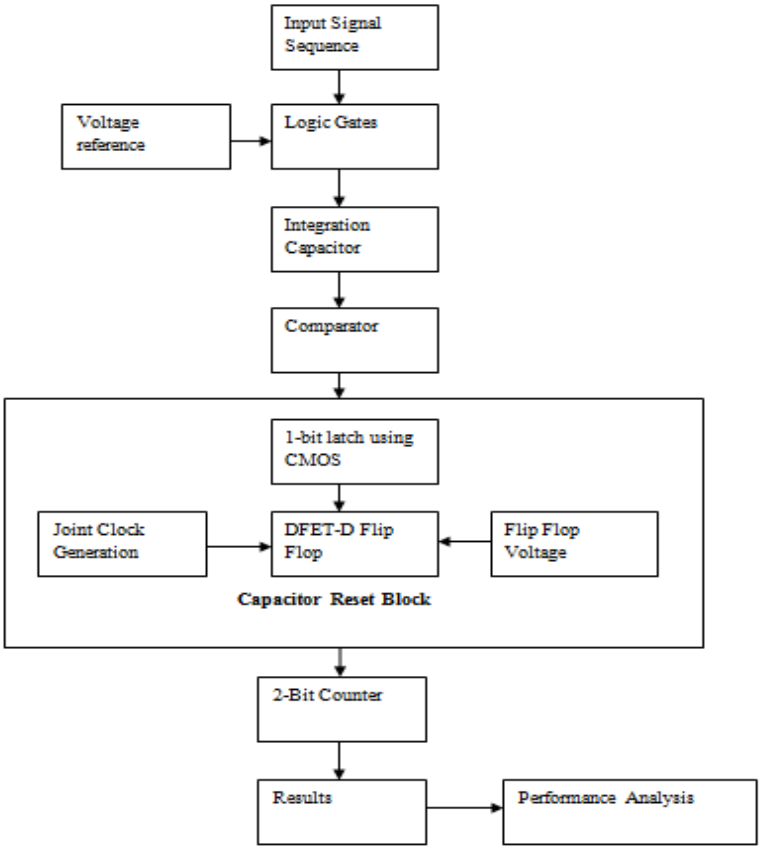

Figure 1. Flow diagram of proposed ROIC

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The above diagram shows the workflow of proposed ROIC. In this system the input signal is given to the integration capacitor and whenever the integration capacitor output voltage exceeds reference voltage during the integration period, the comparator output becomes 1. Then this comparator output reaches the capacitor reset block. The DFET DFF in this block generates the capacitor reset signal at the rising edge as well as at the falling edge of the clock signal. When the comparator output becomes 1 just before the rising edge of the clock signal, the reset signal is generated immediately at the rising edge of the clock signal and if the comparator output becomes 1 after the rising edge of the clock signal then the reset signal is generated at the falling edge of the clock signal. The result of the counter is taken for performance analysis.

III. RESULTS AND DISCUSSION

Here in this work circuit was designed using a 0.18-µm 1-poly 6-metal CMOS process. Measurement result indicates that it has a dynamic range of 99.2 dB with a good signal to noise ratio for a wide range of input signals. Efficiency of the clock-gating technique is verified with the power consumption evaluation. For the same, asynchronous clock-gating technique is employed. Then results were compared to those by the conventional ROICs. This comparison made with 10-MHz and 20-MHz clocks, DET DFF. In this work Power consumed ROIC can be reduced to 75.4% and 42.9% than conventional ROICs Further, in the case of a low input-signal current (high-gain mode), the power consumed by this ROIC in which in this work carried out can be reduced to 2.3% and 1.4% of that consumed by the existing ROIC.

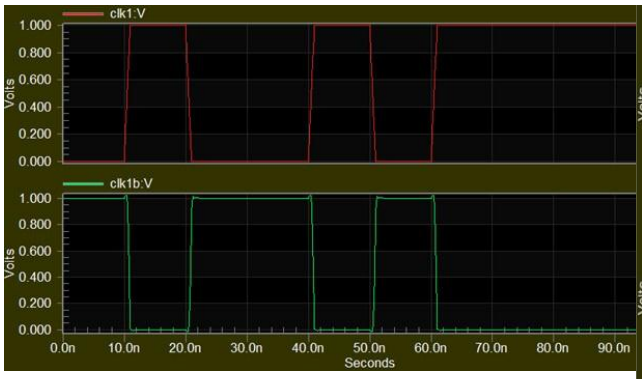

Figure 2. Source Input voltage and output voltage TDF DFF

Clk1:V is low clock voltage, in this the latch is in sample mode.

Clk1b:Vis high clock voltage, in this the latch is in hold mode.

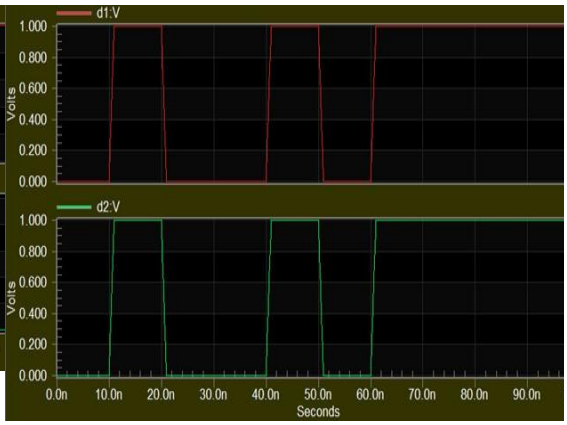

Figure 3. Waveform d1v and d2v are redundant data voltage determined by the 2-1 MUX

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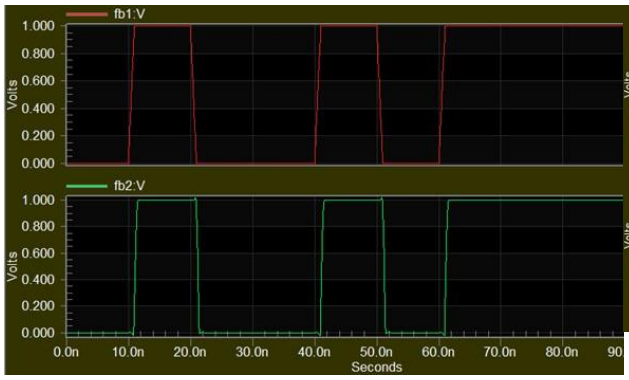

Figure 4. Fb1.V and Fb2.V are Redundant feedback voltages of the feedback nodes in latch.

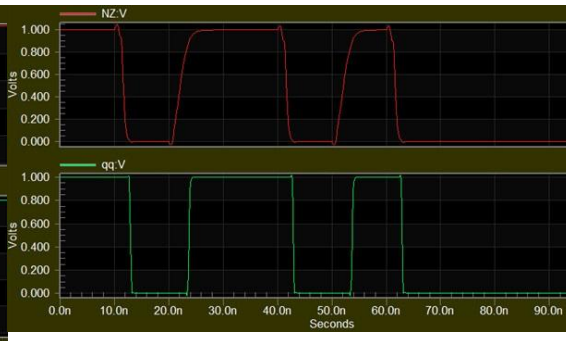

Figure 5. Voltage at internal nodes (NZ:V) and output voltage of the latch(qq:v)

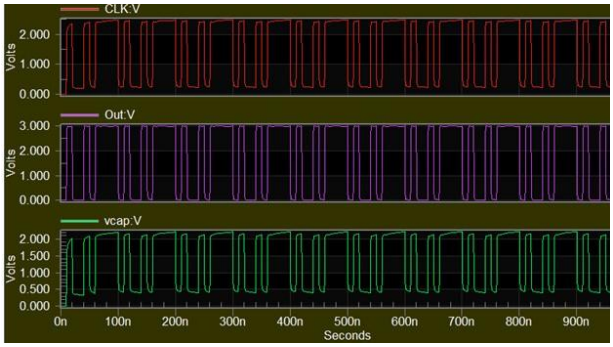

Figure 6.Simulation results of Capacitor-reset block with DEFT-DFF (10-MHz clock)

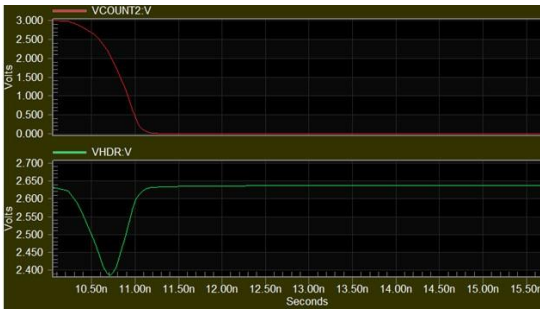

Figure 7. Counter Results-1

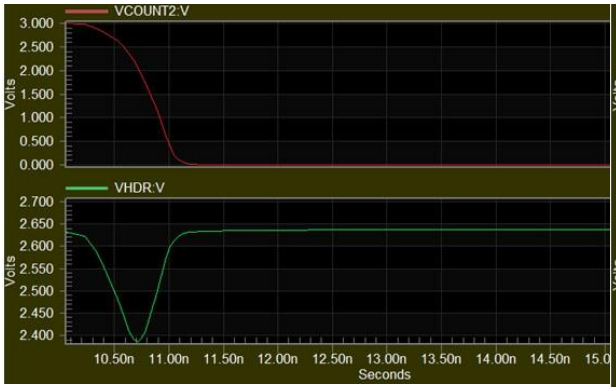

Figure 8. Counter Results - 2

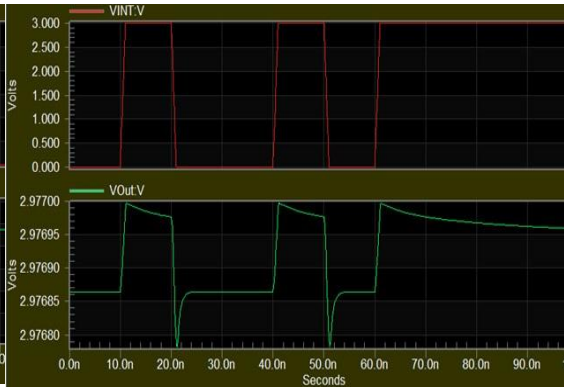

Figure 9. Final input and output of the proposed Readout Integrated circuit (ROIC).

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Table 1. Comparative analysis of Existing and Proposed System

Parameters	Existing SET-DFF 10 MHz	Existing SET-DFF 20 MHz	Existing ROIC(DET-FF)	Proposed ROIC(DFET-FF)
Array Size	128×128	128×128	128×128	128×128
Pixel Pitch	15µm	15µm	15µm	15µm
Full Well Capacity	20×10^6 e-	20×10^6 e-	20×10^6 e-	20×10^6 e-
Dynamic Range	99.2 dB	99.2 dB	99.2 dB	99.2 dB
Delay	66.7uv	33.3uv	33.3uv	16.73uv
Power Consumption(High gain mode)	1.388mW	2.352mW	0.32mW	0.049028mW
Leakage Current	90µA	75µA	75µA	60µA

In this system, delay is 96.46% reduced compared to ROIC in existing system. The power consumption of the proposed ROIC is 74.91% more efficient than the existing system and the leakage current of the proposed ROIC is 33.33% efficient compared to the existing system. Merits of Proposed System are listed as: i) This technique is used to reduce the energy consumption level and to optimize the writing in the D memory functions. ii) Proposed ROIC has low-noise and low-power characteristics with high dynamic range. iii) This system is used to reduce the circuit complexity level.

IV. CONCLUSION

This paper has verified the usefulness of a DFET-DFF-furnished with high dynamic-range ROIC. This ROIC employed the asynchronous clock-gating technique. The DFET-DFF-equipped capacitor-reset block serves to reduce the errors within the final output signal. Here the asynchronous clock gating technique could reduce the power consumed by the ROIC where this work carried out is roughly around 2% of that consumed by conventional ROICs. The proposed ROIC can be considered useful in missile-application systems requiring a high dynamic range of operation, low power consumption, and high sensitivity. This work has shown that how temporal and spatial hardening techniques influence the SEU sensitivity of DFFs as a function of a wide supply voltage range. From results it should be observed that temporal hardening has an increasing effect on the SEU sensitivity. DFF used in this work having increasing supply voltage and decreasing LET. Also, spatial hardening has increased the effectiveness of sensitivity of the DFF. This is happened with decreasing supply voltage and increasing LET. This work has also shown that temporal and spatial SEU hardening techniques in conjunction with supply voltage scaling can be used to realize low power, SEU tolerant circuits. In applications where energy efficiency is prioritized prior to operating frequency, the proposed DFF topology may be well suited for implementation. As a result, SEU cross-section of below cm bit may be achieved with an increased energy efficiency of up to 95%, compared to a DICE DFF at 1 V supply voltage. Higher radiation tolerance may be achieved by separating the sensitive nodes.

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