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SUB-THRESHOLD CIRCUIT USE FOR FULL CUSTOM CELL DESIGN ANALYSIS

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ABSTRCT: The sub threshold method is very important in the current scenario. By the use of sub threshold techniques the circuits can be designed. Keeping this in mind, In this paper the work is done in the sub threshold technique. The sub- threshold logics work on the principle that the MOSFET is operating in region of sub-threshold and for switching purpose it use leakage current in same region, so that it decreases significant amount power. This paper shows the various analysis and assessment of distinct topologies in the region of sub-threshold. This paper showed that how the consumption of power can be reduce. For less consumption of power of sub-threshold circuits the new body biasing technology is designed. The body biasing effect is totally depends on the operation of MOS devices along with proper substrate bias, which deviate due to deviation in voltage of gate. This happens when in NMOS the connection of positive bias voltage is between substrate and gate and in PMOS the connection of negative bias voltage is between substrate and gate. This body biasing technology brings down the dissipation of power and operating current, without any alteration in endure characteristics.

In this paper four distinct topologies are selected and after that designed in the operation of sub-threshold region further this design go through the comparison between the active drain current and leakage current. By using TSPICE for .18um technology the simulation done of sub-threshold structures and conventional structure.

KEYWORDS: Sub- threshold, Dynamic threshold MOS Inverter, Body-biasing.

I. INTRODUTION-

In the case of dissipation of IC power includes the effect of various components which depends on the circuit operations. The powerful method to save power is voltage scaling because of digital circuit's square law.

In the sub-threshold circuits the supply voltage i.e. VDD is less than the Vth of the transistors. The load capacitances leakage current charges and discharges also limits the results but gives the good result in saving the energy in the normal VDD operation. The transistor operation is below the threshold voltage in the operation region of sub-threshold. The benefits of transistor operation below the threshold voltage is shown in the research of sub-threshold region of operation.

Areas of Uses -Digital sub-threshold circuits are used in:-

a) Low power applications.
b) Wristwatches
c) Hearing aids
d) Pacemakers
e) Wireless communication systems.

The significant advantage of ultra-low power is in medical equipments like pacemakers, Hearing aids etc and the equipments which is of low processing requirements.

II. EFFECT OF BODY BIASING –

In the threshold voltage equation the body bias effect can be taken as

The effect of body bias can be considered in the threshold voltage equation as $\mathbf{Vth = VFB + 2_B+[2_{si}*q*N_{cheff}(2_B -V_{BS})]/ Cox}$

To change the body potential can be done in two different ways -

1 **Forward Body Bias-** In this technique to increase the active drain current there is to scale down the threshold voltage.

2 Reverse Body Bias- Reverse-body bias use to increase the threshold voltage of transistors in the STANDBY state for decreasing the leakage current

There are four techniques-
(a) Standard DT-CMOS.
(b) DT-MOS with augmenting devices.
(c) Another topology of DT- CMOS with augmenting devices.
(d) DT-CMOS with Drains connected to substrate.

The threshold voltage of DTMOS which is body contacted transistor is controlled through the connection of the body with the gate. In this way FBB produced to decrease the threshold voltage and like this there is scale up in the active drain current. Other technique named DT-MOS with augmenting devices. In this there is disadvantage that there is not the RBB effect. So that there is not any reduction of the leakage current.

In the second technique this drawback is overcome. In this technique for augmenting devices one NMOS and one PMOS is used, so that they creates the effect of FBB which scale down the threshold voltage and scale up the active drain current and RBB effect. RBB effect increases the threshold voltage of the transistors in the STANDBY state and like this scale down the leakage current.

The third topology is DT- CMOS with augmenting devices which is vary from the previous topologies.

And last DT-CMOS with Drains connected with substrate technique. In this technique to produce the body biasing effect the drain terminal is connected with their substrate of the transistors.

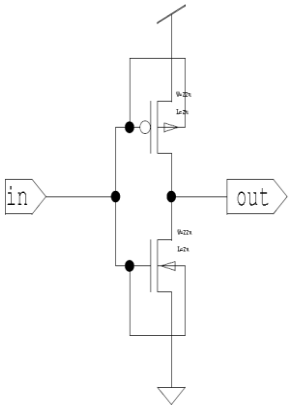


Fig-2(a)

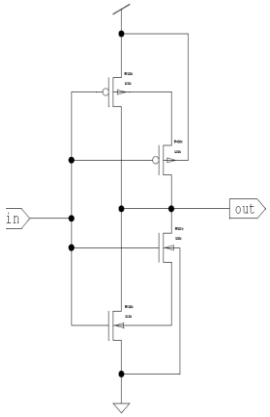


Fig-2(b)

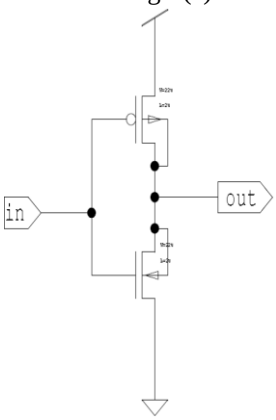


Fig-2(c)

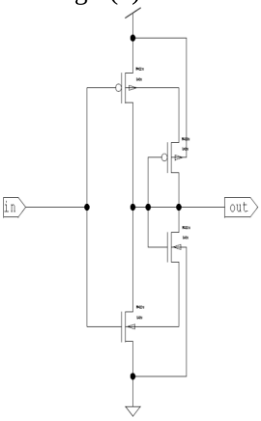


Fig-2(d)

Fig 2(a) Standard DT-CMOS
Fig 2(b) DT-MOS with augmenting devices
Fig 2(c) Another topology of DT- CMOS with augmenting devices

Fig 2(d) DT-CMOS with Drains connected.

III. SIMULATION RESULTS-COMPARISON OF ACTIVE DRAIN CURRENT BETWEEN DIFFERENT TOPOLOGIES –

ID	Transistors	BASE	DTMOS	AUG DVC	ANTR TOP	DRAIN CO
	M1					
0	M2	-2.28E-11	-1.16E-11			-5.45E-11
PMOS	M3			-3.31E-10	-7.85E-11	
	M4			1.92E-11	-1.68E-12	
	M1	2.38E-11	9.76E-12	-3.25E-11	4.13E-11	-2.22E-11
	M2			2.47E-10	3.65E-12	
NMOS	M3					
1	M4					

Comparison of Leakage Current between different topologies –

Leakage ID	Transistors	BASE	DTMOS	AUG DVC	ANTR TOP	DRAIN CO
	M1	2.10E-11	5.21E-12	5.76E-13	4.14E-11	5.35E-11
0	M2			2.79E-11	2.94E-12	
NMOS	M3					
	M4					
	M1					
PMOS	M2	-1.67E-11	-3.38E-12			-8.97E-11
	M3			-4.10E-11	-6.98E-11	
1	M4			-4.75E-13	-2.07E-12	

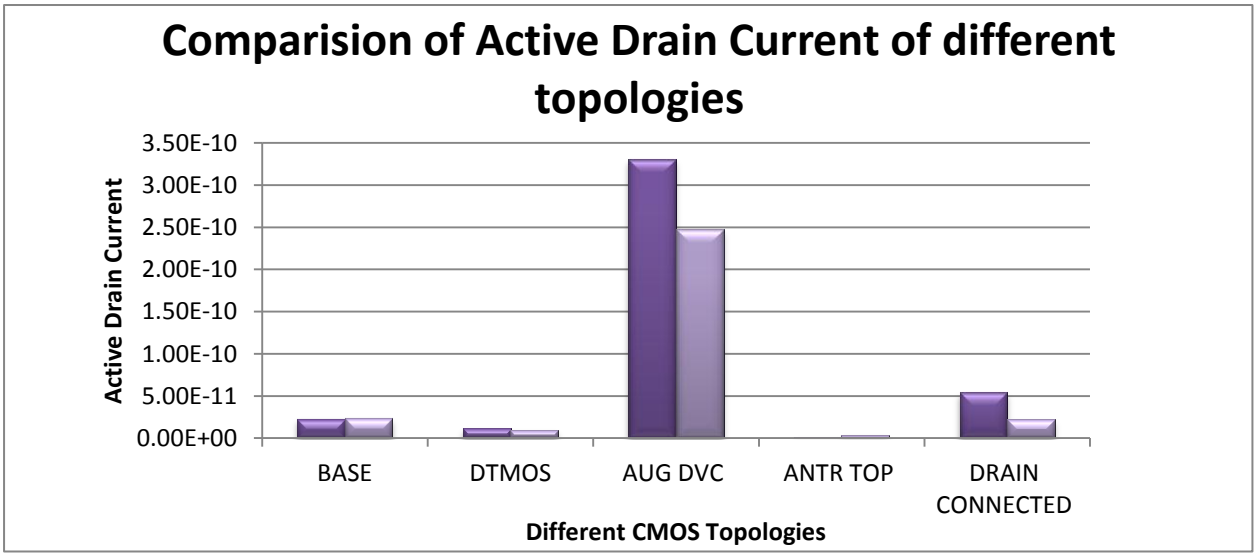
Creating Library cells- As we found that in all four techniques Augmenting devices technique is the best. So we are developing library cells which includes NAND, NOR.

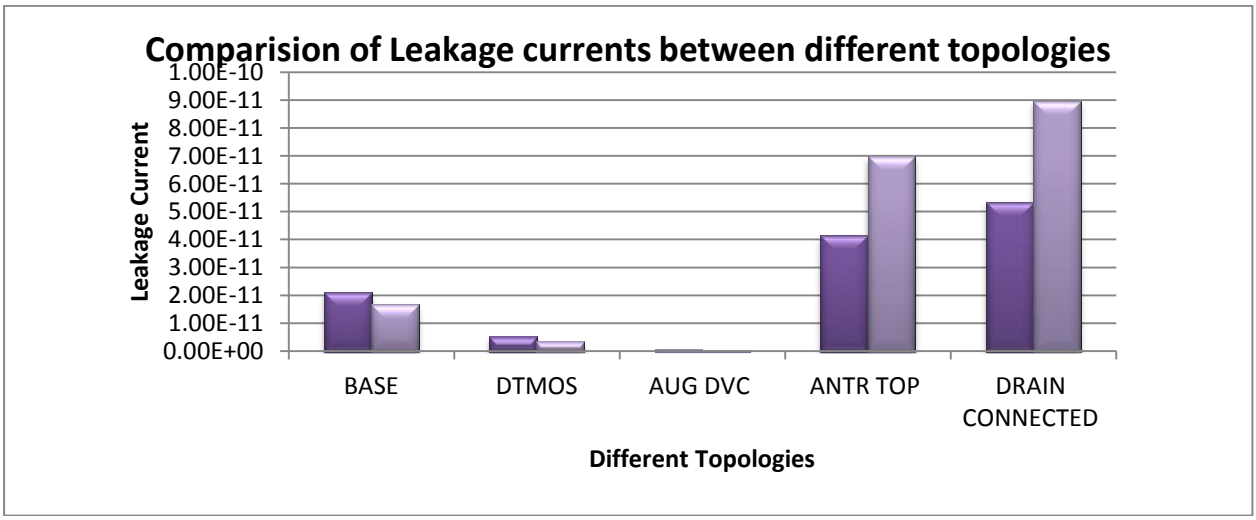
SIMULATION TABLE FOR NAND GATE

INPUT		TYPE	ID	VGS	VDS	VBS	VTH	Vout
11	M1	NMOS	3.43E-10	1.85E-01	2.23E-02	3.91E-02	4.70E-01	
	M2	NMOS	-3.23E-10	1.63E-01	-2.10E-02	2.05E-02	4.70E-01	
	M3	NMOS	-2.53E-10	1.46E-01	-3.78E-02	-3.91E-02	4.80E-01	
	M4	NMOS	-2.77E-10	1.42E-01	-4.14E-02	-4.27E-02	4.80E-01	1.30E-03
	M6	PMOS	6.91E-13	0.00E+00	1.29E-02	-6.55E-02	-4.66E-01	
	M7	PMOS	-7.34E-13	6.55E-02	-1.18E-01	6.55E-02	-5.06E-01	
	M8	PMOS	-4.65E-13	9.30E-02	-9.07E-02	9.30E-02	-5.15E-01	

SIMULATION TABLE FOR NOR GATE

INPUT		TYPE	ID	VGS	VDS	VBS	VTH	Vout
11	M1	NMOS	-3.27E-11	1.62E-01	-7.37E-03	-2.33E-02	4.84E-01	
	M2	NMOS	1.92E-10	1.85E-01	1.60E-02	2.33E-02	4.74E-01	
	M3	NMOS	1.92E-10	1.85E-01	1.60E-02	2.33E-02	4.74E-01	1.60E-02
	M4	NMOS	-3.27E-11	1.62E-01	-7.37E-03	-2.33E-02	4.84E-01	
	M5	PMOS	-1.20E-11	0.00E+00	-3.86E-02	-6.01E-02	-4.71E-01	
	M6	PMOS	-1.10E-11	3.86E-02	-1.30E-01	-5.66E-02	-4.70E-01	
	M7	PMOS	-7.74E-13	6.01E-02	-1.09E-01	6.01E-02	-5.05E-01	
	M8	PMOS	-3.93E-13	9.52E-02	-7.38E-02	9.52E-02	-5.16E-01	





IV. CONCLUSION-

After studying all the results the conclusion find is that the DT-CMOS with augmenting devices is the best sub-threshold technique among all the other techniques. It produces FBB and RBB at the same time. The RBB decreases the leakage current and FBB increases the active drain current.

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