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DESIGN OF HIGH PERFORMANCE FREQUENCY MULTIPLIER FOR DLL BASED PULSE GENERATOR

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ABSTRACT:

Major operation block in any processing unit is a multiplier. There are many multiplication algorithms are suggested, by using this algorithms multiplier structure can be designed. With the advancement of technology, demand for circuits with high reliable and high speed is increasing. So, A high-speed and highly reliable DLL (Delay-Phase Locked Loop) based pulse generator frequency multiplier is presented in this paper. This multiplier structure initially performs partial product generation from multiplier and multiplicand. Then the frequency multiplying technique is performed by using an edge combiner based clock synthesis system, which can achieve a high-speed and highly reliable operation using a hierarchical structure and an overlap canceller. In addition, by applying the logical effort to the pulse generator and multiplication-ratio control logic design, the presented frequency multiplier minimizes the delay difference between positive and negative-edge generation paths, which causes a deterministic jitter. The final addition stage of partial products is performed by parallel prefix adder (PPA). The presented frequency multiplier is fabricated using a 0.13-µm CMOS process technology and an output range of 100 MHz–3.3 GHz. The presented designs can be analyzed with respect to traditional multiplier design in terms of jitter, area and power consumption.

KEYWORDS: DLL (delay-phase locked loop), frequency multiplying technique, edge combiner, parallel prefix adder (PPA).

I. INTRODUCTION

The frequency multiplier is an electronic circuit that produces an output signal whose frequency is an integral multiple (harmonic) of its input frequency. Frequency multiplier contains a nonlinear circuit that alters the input signal and produces harmonics of that signal [1]. A band pass filter selects the desired fundamental frequency and removes the unwanted harmonics from the output.

Frequency multipliers find a wide variety of applications in nonlinear optics to generate various harmonics of laser light, telecommunication circuits for instrument processing, frequency synthesizers and circuit analysis in analog processing [2]. It can be more conservative to build up a lower frequency signal with lower control and after that utilization of the frequency multiplier to create an output signal having a frequency in millimetre or microwave range. Also, oscillators designed with the help of frequency multipliers have simplified design and improved phase noise. Power has turned out to be a standout amongst the most critical worries in plan merging for multi gigahertz correspondence frameworks, for example, optical information joins, remote items, chip, and ASIC/SOC outlines. Power utilization has turned into a bottleneck in chip plan. With an end goal to decrease the power consumption of the circuit, the

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supply voltage can be diminished prompting lessening of dynamic and static power dissipation. Bringing down the supply voltage likewise lessens the execution of the circuit, which is usually unsatisfactory [3].

Phase Lock Loop (PLL) is a closed-loop feedback system that is used to fix constant phase relationship between its reference clock phase and the phase of the output clock [4]. PLL is an essential analog circuit having various communication applications such as clock generation, frequency synthesizer, clock recovery, radio, computer, etc. Phase Locked Loops are mainly utilized for clock synthesis, synchronization, skew and jitter reduction. PLLs are also used to produce all around coordinated on-chip checks in elite computerized frameworks [5]. In order to reduce the overall power dissipation of the circuit, phase lock loop architecture is used for designing frequency multipliers. In a PLL the voltage controlled oscillator (VCO), when combined with a divider in the feedback path then it can run at desired multiples of the reference frequency. The synthesizer frequency in this paper employs a DLL [6]. Due to the different configuration, DLLs are preferred for their unconditional stability and faster locking time than PLLs. Also the delay lines of DLLs introduce much less jitter than the oscillators which are necessary for PLLs. The noise injected into a DLL disappears at the end of the delay line, whereas it is recirculated in an oscillator. Thus DLL are practically considered suitable for clock multiplication applications, because of DLL provide lower jitter than PLL [7].

A high-speed and highly reliable DLL (Delay-Phase Locked Loop) based pulse generator frequency multiplier is going to be presented in this work. The DLL provides multi-phase signals, which feeds to the frequency multiplier. Then, frequency multiplier enables multiplying the frequency of input signal without a jitter accumulation problem. Multiplication factor N/2 (N=integer) of the proposed frequency multiplier can be chosen easily according to the number of delay cell. Owing to the suggested edge combiner, this frequency multiplier can generate a higher frequency and wider frequency range multiplied clock with a lower power consumption per frequency ratio and higher reliability than previous frequency multipliers [8].

II. DELAY PHASE LOCKED LOOP

While operating high-frequency and high performance electronic systems, the problems encountered in the distribution of clock signal throughout entire system. An external clock cannot be used, thus creating the need for an on-chip clock multiplier for high speed products. Both the phase-locked loops (PLLs) and the delay-locked loops (DLLs) have been employed. Delay-locked loops (DLLs) can be considered as feedback circuits that phase lock an output to an input without the using an oscillator. In some applications, DLLs are necessary or preferable over phase-locked loops (PLLs), with their advantages including lower sensitivity to supply noise and lower phase noise.

This paper presents high complication and time-varying workload of developing multimedia applications possess a major challenge for (DVS) algorithms [9]. For real time application many DVS algorithms have been presented which is productive method to classify such DVS algorithms by excellent multimedia application which does not exist. In this paper, they

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suggest the new offline linear programming method to regulate the low energy utilization for processing multimedia tasks under delay deadlines. On the basis of the accessed energy lower bound, they analyzed excellence of DVS algorithms. Afterword, they boost the LP formulation in order to construct an online DVS algorithm for real-time multimedia processing based on powerful sequential linear programming.

The traditional voltage escalating system is studied in the paper [10] that requires a delay margin to continue a certain level of firmness across all possible device and wire process deviations and temperature inconsistency. This margin is required to canvas for a possible change in the critical path due to such changes. Moreover, a critical path changes from one operating voltage to another due to slower interconnect delay that arises with voltage compared to logic delay. To assure a fault free operation with high limit both process variation and interconnect delay are in challenging with technology scaling. Such margin is provided into voltage upward and corresponding energy inadequately. Moreover, voltage scaling characteristics of the certain critical path is firmly followed by programming logic and interconnects delay lines to carry out same delay sequences as the actual critical path.

A delay-locked loop (DLL)-based frequency synthesizer is designed [11] for the ultra-wideband (UWB) Mode-1 system. This frequency synthesizer achieves less than 9.5-ns settling time with appropriate 528-MHz input reference frequency. This reference frequency utilizes wide loop bandwidth and rapid selling architecture. Furthermore, a discrete-time model and an analytical model of the DLL are anticipated here for phase noise in this work. Investigational results show great reliability with predicted settling time and phase noise. Previous works presented many types of high frequency clock generators based on DLL [12]. A DLL based local oscillator for personal communications service applications has used an edge combiner for frequency multiplication. However, it requires an LC tank, which consumes a large chip area. Also, the frequency multiplication ratio is fixed once the LC-tank component values are chosen. In [13], a DLL-based frequency synthesizer used AND-OR gates and programmable DLL based frequency multiplier used latch gates for frequency multiplication. However, digital logic gates are very sensitive to power supply noise, which significantly affects the peak-to-peak jitter performance.

In the paper [14], a delay-locked loop (DLL)-based clock generator is presented has several inherent advantages over conventional phase-locked-loop-based generator, i.e, no jitter growth, quick locking, balanced loop production and easy combination of the loop filter. DLL based clock generator requires a fresh reference signal. To conquer limited locking range and frequency multiplication problem of the conservative DLL-based system here they suggest a phase detector with reset circuitry and a novel frequency multiplier. The die area, peak-to-peak, and R.M.S. jitter are the three smallest comparison parameter which is related to those of high-frequency clock multipliers.

In the paper [15] they survey, the microprocessor system in portable electronic devices often has a time-varying computational load which is comprised of: (1) Figure out rigorous and

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stationary processes, (2) surroundings and high-latency processes, and (3) structure found idle. The fundamental design objectives for the processor systems in these applications are supplying the highest possible peak performance for the compute-intensive code while maximizing the battery life for the remaining low performance periods.

III. DLL-BASED PULSE GENERATOR FREQUENCY MULTIPLIER

The presented DLL-based clock generator is composed of a DLL core and the presented frequency multiplier, as shown in Fig. 1. This frequency multiplier is composed of pulse generator, multiplication-ratio control logic, and an edge combiner. To enhance the lock time, which is an important design parameter in the clock generator, a dual-edge-triggered phase-detector-based DLL (DET-PD DLL) core is adopted.

3.1 Partial Product Generation

Partial products are generated with the help of AND gates. The partial products are generated with the help of easy multiples of X, 2X, 4X, 5X. Each bit of multiplier and multiplicand are multiplied first by performing AND operation between multiplier and multiplicand bits say A and B respectively. The partial products can be calculated as follows,

Partial Products= A_i AND B_i

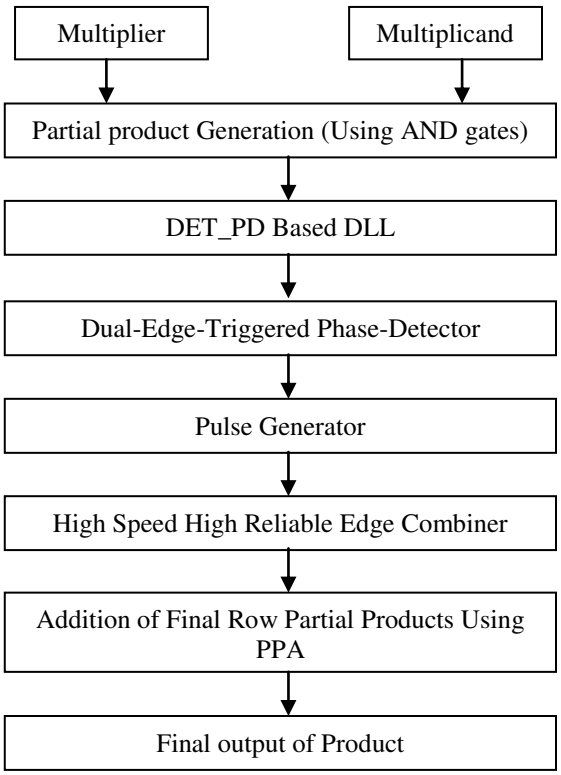

Fig. 1: BLOCK DIAGRAM OF HYBRID ADDER

3.2 DET-PD based DLL

The lock performance can be improved by comparing the signals at both positive and negative edges of reference signal and output of feedback signal. This can be done by Dual edge

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triggered phase detector. An ideal DET PD achieves same throughput with half of the clock frequency compared to single edge triggered phase detector. It effectively reduces the power consumption in the clock distribution network. The dual-edge-triggered phase-detector compares both the positive and the negative edges of CLKREF, DCK, CLKOUT and DCK which are the duty cycle recovered clocks of CLKREF and CLKOUT using the duty-cycle keeper. The DLL is locked within 300 cycles in all process-voltage-temperature corners owing to the dual-edge detection characteristic, and generates 32-phase differential clocks (CLK0:32 and /CLK0:32).

3.3 Pulse Generator

The pulse generator generates the appropriate number of pulses from the multiphase clocks according to the multiplication-ratio control signal, and the edge combiner generates a multiplied clock using the selected pulses. Using the 32-phase differential clocks, the pulse generator makes pulses (PG0:31 and /PG0:31) for positive edge and negative edge generation. The multiplication-ratio control logic selects appropriate pulses from PG0:31 and /PG0:31 and generates MCP, 0:15 and MCN, 0:15 according to the multiplication-ratio control signal. The pulse generator and the multiplication-ratio control logic structures have an optimized design to match the delay between the positive-edge and negative-edge generation paths of the multiplied clock. Owing to these pulse generator and multiplication ratio control logic structures, the positive and negative-edge generation paths of the multiplied clock have the same structures (two NAND gates, two NOR gates, one tri-state inverter, and one inverter). Because both the paths have the same path logical effort, they can be designed to have the same delay and thus, the deterministic jitter can be minimized.

3.4 High-Speed and Highly Reliable Edge Combiner (HSHR-EC)

HSHR edge combiner is used to solve the speed and reliability issues of the previous edge combiner, for this purpose presented the pre-combining, overlap canceller, and push-pull stage to enhance multiplied clocks. Finally, the high-speed and highly reliable edge combiner (HSHR-EC) generates one multiplied clock (CLKMUL) using all the outputs of the multiplication ratio control logic. Since the number of multiphase is 32, the maximum multiplication ratio is 16. HSHR-EC consists of a pre-combining stage, overlap canceller, and push–pull stage. The two-step edge combiner, pre-combining, and push–pull stage are used to enhance the maximum multiplied clock frequency. The overlap canceller is used to guarantee the stable operation of the frequency multiplier. As the number of signals merged in the pre-combining stage (NPRE) increases then the number of PU-Ps and PD-Ns required in the push–pull stage are reduced by a factor of NPRE. It might appear that, by increasing NPRE, the maximum multiplied clock frequency of the HSHR-EC can be enhanced; however, because the logic depth and the number of NAND and NOR gates in the pre-combing stage are equal to log2NPRE and 32(1–1/NPRE), respectively, a large NPRE causes the pre-combining stage to be vulnerable to process variation, which in turn can cause a large deterministic jitter. Thus, NPRE is limited to two, which corresponds to a logic depth of one in the HSHR-EC, and thus, the pre-combining stage can be simply realized using NAND and NOR gates

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3.5 Addition of Final Row Partial Products Using PPA

The straight and simply forward approach to implement the PPA is Brent kung adder to adopt pairing of the two partial products at the same time, summing them with the use of an adder and repeat the complete process until just the final result is left. If a single adder is used to perform all these operations, then this partial product reduction technique will take N-cycles which mean a grand total of N mechanical delays when the relay adder is used.

Brent Kung Adder: The Brent Kung adder scheme uses 2-bit groups to compute the prefixes. They are further used to compute 4-bit group prefixes, which are in turn then used for the computation of 8-bit group prefixes. The process is similarly carried on to further find the higher bit prefixes. The output carry of a particular bit stage is obtained using these prefixes. To obtain the Sum bit of a particular stage, the output carry is used along with the next stage group propagate signal.

3.6 Final Output of Multiplier

A carry save adder is used to accumulate the partial products which resulting in the final sum and carry. It improves the accumulation speed of the partial product as it saves the carry and passes it to the next level of carry select adder. Therefore, the adders in the same layer become independent of each other and can be executed simultaneously. Hence the time required for the addition operation is reduced. Accumulation is combined with a carry save adder tree to compress the partial products.

IV. RESULTS

The present DLL based phase generated frequency multiplier is implemented using a DET-PD based DLL in 0.13-μm CMOS process technology, and has a supply voltage of 1.2 V. The overall test chip occupies an active area of 0.037mm^2, and the presented frequency multiplier has the multiplication ratios of 1, 2, 4, 8, and 16, and a maximum multiplied clock frequency of 3.3 GHz. Because the minimum operating frequency of the DLL core is 100 MHz, the multiplied clock frequency has a range from 100 MHz to 3.3 GHz. At 3.3 GHz, the overall DLL-based clock generator consumed 24.7mW.

Table 1 presents a comparative analysis of performance between PLL based, DLL based and the presented DET-PD based DLL frequency multipliers. The presented DLL offers higher multiplication factor and wider operating frequency range compared to others. It provides a good jitter performance for a high multiplication factor. The power consumption is also reasonable compared to PLL and DLL based frequency multipliers.

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TABLE 1: COMPARATIVE ANALYSIS OF PERFORMANCE

Parameter	**PLL**	**DLL**	**DET-PD based DLL**
Power Supply	1.8V	1.8V	1.2V
Frequency range	100-640MHz	232MHz - 1.5GHZ	100MHz - 3.3GHz
CMOS Technology	180nm	0.18 µm	0.13 µm
Power Consumption	140mW	54mW @3.4GHz	24.7mW @3.3GHz
Architecture	PLL	EC	DET-PD based DLL+EC
Max. Multiplication ratio	NA	4	16
Area	0.19 mm^2	0.337m m^2	0.037m m^2
jitter	19ps	16.37ps	13.6ps

Figure 2 shows the comparative analysis of area performance. As an overall trend, the DET-PD based DLL multiplier architecture has a competitive performance and achieves the lowest area consumption compared to the other architectures.

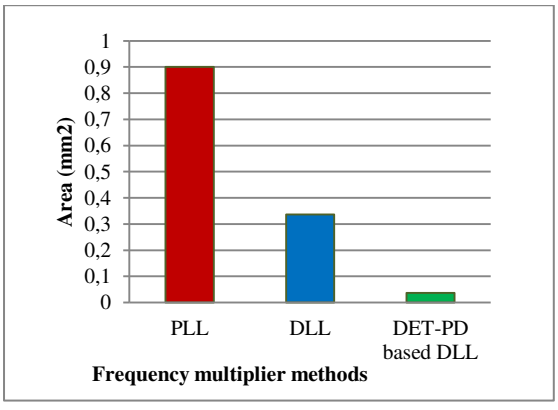

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Fig. 2: COMPARATIVE ANALYSIS OF AREA PERFORMANCE

Figure 3 shows the comparative analysis of jitter performance. As shown in Fig. 3, the DET-PD based DLL multiplier architecture has a low jitter of 13.6ps compared to the PLL based multiplier of 18.37ps and DLL based multiplier of 16.37ps competitive performance.

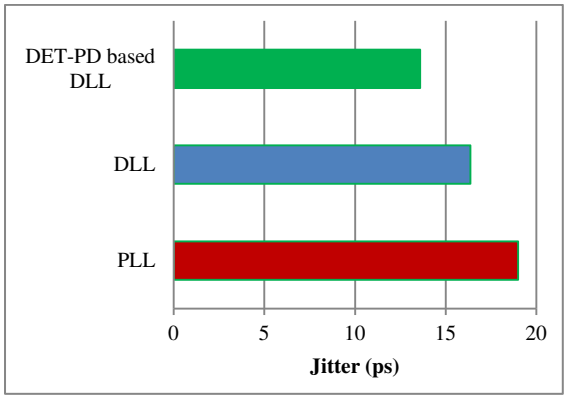

Fig. 3: COMPARATIVE ANALYSIS OF JITTER PERFORMANCE

The jitter decreases as the multiplication ratio decreases, because the jitter induced by the delay cell mismatch in Voltage Controlled Delay Line (VCDL) reduces. Instead, jitter is largely dependent on DLL reference clock frequency. Because the VCDL generates one period delay of DLL reference clock, the slope of the clocks in VCDL should be degraded at a low DLL reference clock frequency. Due to this characteristic, jitter increases at a low DLL reference clock frequency.

V. CONCLUSION

In this paper, a DLL based phase generated frequency multiplier has presented. This multiplier structure used a HSHC-EC that guarantees high-speed operation owing to its hierarchical edge-combiner structure and highly reliable operation owing to its use of an overlap canceller. The optimized pulse generator and the multiplication-ratio control logic are presented to reduce the delay difference between positive and negative-edge generation paths. Final stage of multiplier employed Brent Kung PPA adder that provide low delay and area. The frequency multiplier is fabricated using the 0.13μm CMOS process technology. This circuit can operate with the supply voltage of 1.2V. The power consumption is 24.7mW. The DLL core cycle to cycle jitter is 13.6ps. Therefore presented multiplier structures can be used in high speed and low area application circuits.

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