Toll-Gate Payment Automation with RFID and SMS Alerts

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***Abstract*—** RFID is used for reading the physical tags on single products, cases, pallets, or re-usable containers which emit radio signals to be picked up by reader devices. The complete RFID picture combines the technology of the tags and readers with access to global standardized databases. This project is to make the payment automation in toll gate using RFID technology. Here the process is worked out by using microcontroller along with GSM modem. Whenever the vehicle enters the toll gate, the vehicle is detected automatically through the RFID card present with owner. To read the information from RFID card, RFID reader is available at toll gate. Here we have to design one circuit with the help of RFID reader, GSM module, LCD, L293D, DC motor and external memory. Here DC motor is used as a toll gate. Whenever user is placing RFID card nearer to RFID reader it will read the information from the card and give it to microcontroller. Now microcontroller read the card number and it will check whether card is valid or not. If that card is valid some amount is reduced from user account and one message is transmitted to the user with the help of GSM module. The message contains how much amount is reduced from the user account. The resultant amount is stored in the external memory.

***Index Terms*— RFID, ATmega162, GSM SIM300.**

I. INTRODUCTION

Radio Frequency Identification (RFID) is evolving as a major technology enabler for identifying and tracking goods and assets around the world. It can help hospitals locate expensive equipment more quickly to improve patient care, pharmaceutical companies to reduce counterfeiting and logistics providers to improve the management of moveable assets. It also promises to enable new efficiencies in the supply chain by tracking goods from the point of manufacture through to the retail point of sale (POS). Micro-controllers are useful to the extent that they communicate with other devices, such as sensors, motors, switches, keypads, displays, memory and even other micro-controllers. Many interface methods have been developed over the years to solve the complex problem of balancing circuit design criteria such as features, cost, size, weight, power consumption, reliability, availability, manufacturability Embedded system means the processor is embedded into the required application. An embedded product uses a microprocessor or microcontroller to do one task only. In an embedded system, there is only one application software that is typically burned into ROM. Example: printer, keyboard, video game player

This report describes about the payment at toll-gate using this RFID module, microcontroller and GSM module called block matching motion estimation, which uses matching the blocks with in the frames to estimate the motion.

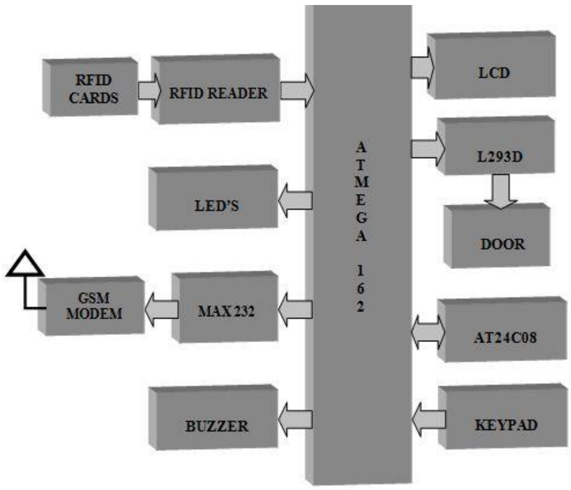

Fig. 1 Block Diagram

II. RFID MODULE

An RFID tag is an object that can be applied to or incorporated into a product, animal, or person for the purpose of identification and tracking using radio waves. Some tags can be read from several meters away and beyond the line of sight of the reader. Most RFID tags contain at least two parts. One is an integrated circuit for storing and processing information, modulating and demodulating a radio-frequency (RF) signal, and other specialized functions. The second is an antenna for receiving and transmitting the signal. Two frequency ranges are generally distinguished for smart RFID systems, High Frequency (HF) 13.56 MHz and Ultra High Frequency (UHF) 860-956 MHz. SATO can support the encoding requirements for both Wal-Mart and Metro following the general epic and ISO regulations.

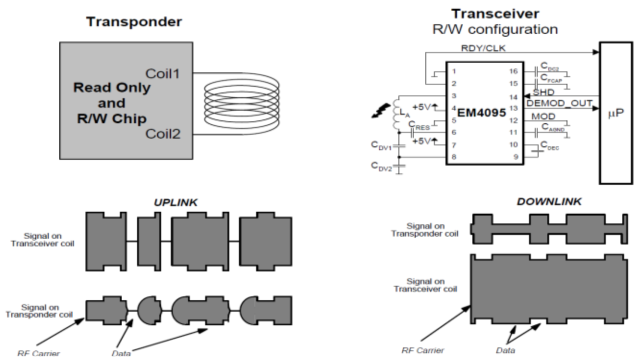

Fig. 2 System Principle

Device operation is controlled by logic inputs SHD and MOD. When SHD is high EM4095 is in sleep mode, current consumption is minimized. At power up the input SHD has to be high to enable correct initialization. When SHD is low the circuit is enabled to emit RF field, it starts to demodulate any amplitude modulation (AM) signal seen on the antenna. This digital signal coming from the AM demodulation block is provided through DEMOD_OUT pin to the microcontroller for decoding and processing. High level on MOD pin forces in tri-state the main antenna drivers synchronously with the RF carrier. While MOD is high the VCO and AM demodulation chain are kept in state before the MOD went high. This ensures fast recovery after MOD is released. The switching ON of VCO and AM demodulation is delayed by 41 RF clocks after falling edge on MOD. In this way the VCO and AM demodulation operating points are not perturbed by startup of antenna resonant circuit The antenna drivers supply the reader base station antenna with the appropriate energy. They deliver current at the resonant frequency which is typically 125 kHz. Current delivered by drivers depends on Q of external resonant circuit.

It is strongly recommended that design of antenna circuit is done in a way that maximum peak current of 250 mA is never exceeded (see Typical Operating Configuration for antenna current calculation). Another limiting factor for antenna current is Thermal Convection of package. Maximum peak current should be designed in a way that internal junction temperature does not exceed maximum junction temperature at maximum application ambient temperature. 100% modulation (field stop) is done by switching OFF the drivers. The ANT drivers are protected against antenna DC short circuit to the power supplies. When a short circuit has been detected the RDY/CLK pin is pulled low while the main driver is forced in tri-state. The circuit can be restarted by activating the SHD pin.

III. MICRO CONTROLLER MODULE

Microcontrollers as the name suggests are small controllers. They are like single chip computers that are often embedded into other systems to function as processing/controlling unit. Many microcontroller designs typically mix multiple interfacing methods. In a very simplistic form, a micro-controller system can be viewed as a system that reads from (monitors) inputs, performs processing and writes to (controls) outputs. In this, two serial communications exists. According to the requirements, ATmega162 microcontroller is best suitable to this project.

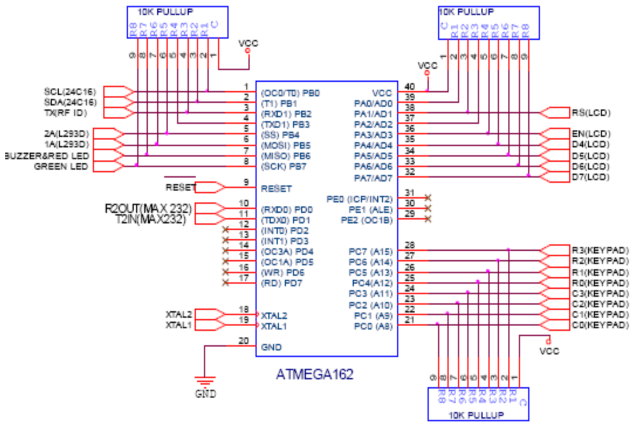

Fig. 3 Schematic diagram to ATmega162 Microcontroller

ATmega162 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega162 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

ATmega162 has two USART's, USART0 and USART1. The functionality for both USART's is described below. USART0 and USART1 have different I/O Registers. Note that in ATmega161 compatibility mode, the double buffering of the USART Receive Register is disabled. Note also that the shared UBRRHI Register in ATmega161 has been split into two separate registers, UBRR0H and UBRR1H, in ATmega162.

IV. LIQUID CRYSTAL DISPLAY

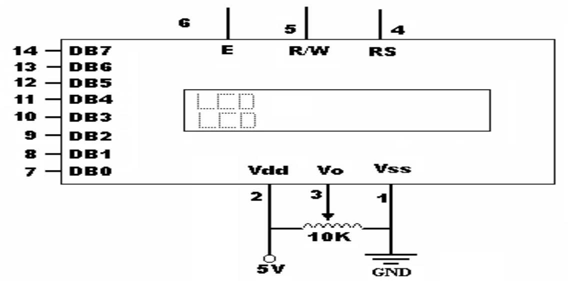

Fig. 4 Pin Diagram of LCD Module

A liquid crystal display **(**LCD) is a thin, flat panel used for electronically displaying information such as text, images, and moving pictures. Its uses include monitors for computers, televisions, instrument panels, and other devices ranging from aircraft cockpit displays, to every-day consumer devices such as video players, gaming devices, clocks, watches, calculators, and telephones. Among its major features are its lightweight construction, its portability, and its ability to be produced in much larger screen sizes than are practical for the construction of cathode ray tube (CRT) display technology. Its low electrical power consumption enables it to be used in battery-powered electronic equipment. It is an electronically-modulated optical device made up of any number of pixels filled with liquid crystals and arrayed in front of a light source (backlight) or reflector to produce images in color or monochrome. speed

V. GSM SIM300 MODULE

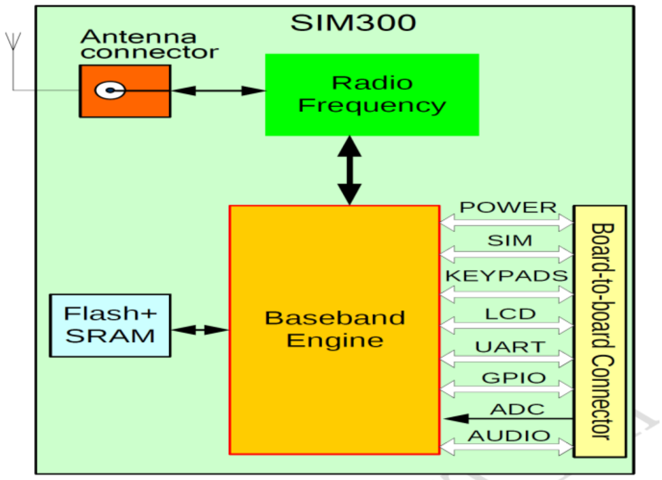

Fig. 5 Functional Diagram of GSM Network

Global system Designed for global market, SIM300 is a Tri-band GSM/GPRS engine that works on frequencies EGSM 900 MHz, DCS 1800 MHz and PCS 1900 MHz. SIM300 features GPRS multi-slot class 10/ class 8 (optional) and supports the GPRS coding schemes CS-1, CS-2, CS-3 and CS-4. With a tiny configuration of 40mm x 33mm x 2.9mm, SIM300 can meet almost all the space requirements in your applications, such as smart phone, PDA phone and other mobile devices. The physical interface to the mobile application is a 60-pin board-to-board connector, which provides all hardware interfaces between the module and customers' boards except the RF antenna interface.

The keypad and SPI display interface will give you the flexibility to develop customized Applications.
Serial port and Debug port can help you easily develop your applications.

Two audio channels include two microphones' inputs and two speakers' outputs. This can be easily configured by AT command.

The SIM300 provides RF antenna interface with alternatives: antenna connector and antenna pad. The antenna connector is MURATA MM9329-2700RA1. And customer's antenna can be soldered to the antenna pad. The SIM300 is designed with power saving technique so that the current consumption is as low as 2.5mA in SLEEP mode. The SIM300 is integrated with the TCP/IP protocol; extended TCP/IP AT commands are developed for customers to use the TCP/IP protocol easily, which is very useful for those data transfer applications.

VI. MAX232

The MAX232 is an integrated circuit that converts signals from an RS-232 serial port to signals suitable for use in TTL compatible digital logic circuits. The MAX232 is a dual driver/receiver and typically converts the RX, TX, CTS and RTS signals the drivers provide RS-232 voltage level outputs (approx. ± 7.5 V) from a single + 5 V supply via on-chip charge pumps and external capacitors. This makes it useful for implementing RS-232 in devices that otherwise do not need any voltages outside the 0 V to + 5 V range, as power supply design does not need to be made more complicated just for driving the RS-232 in this case.

The receivers reduce RS-232 inputs (which may be as high as ± 25 V), to standard 5 V TTL levels. These receivers have a typical threshold of 1.3 V, and a typical hysteresis of 0.5 V.

So a voltage or level converter is needed which can convert TTL to RS232 and RS232 to TTL voltage levels. The most commonly used RS-232 level converter is MAX232. This IC includes charge pump which can generate RS232 voltage levels (-10V and +10V) from 5V power supply. It also includes two receiver and two transmitters and is capable of full-duplex UART/USART communication.

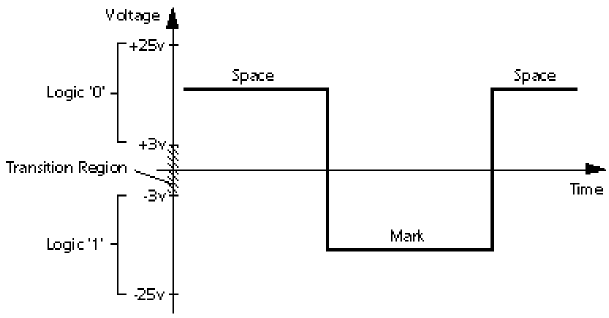

Fig. 6 Voltage levels of MAX232

The later MAX232A is backwards compatible with the original MAX232 but may operate at higher baud rates and can use smaller external capacitors – 0.1 µF in place of the 1.0 µF capacitors used with the original device. Usually all the digital ICs work on TTL or CMOS voltage levels which cannot be used to communicate over RS-232 protocol.

VII. KEYPAD

A keypad is a set of buttons arranged in a block or "pad" which usually bear digits and other symbols and usually a complete set of alphabetical letters. If it mostly contains numbers then it can also be called a numeric keypad. Keypads are found on many alphanumeric keyboards and on other devices such as calculators, push-button telephones, combination locks, and digital door locks, which require mainly numeric input.

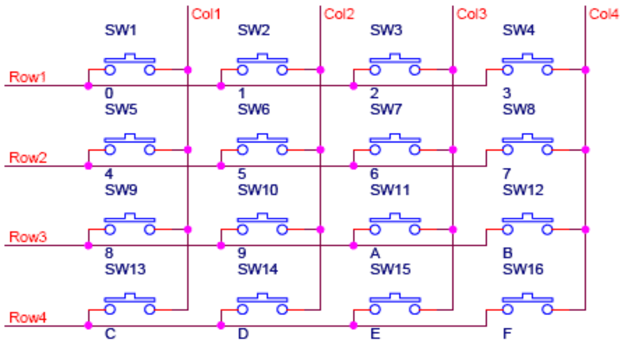

Fig. 7 Schematic Diagram of Keypad

The process of scanning of a key follows the four steps.

1. To make sense that the preceding key has been released, 0's is output to all rows at once and the columns are read and checked repeatedly until all the columns are high. When all columns are found to be high, the program waits for a short amount of time before it goes to the next stage of waiting for a key to be pressed.

2. To see if any key is pressed, the columns scanned over and over in an infinite loop until one of them has a zero (0) on it. Remember that the output latches connected to rows still have their initial zero's making them grounded. After the key press detection, it waits 20ms for bounce and then scans the columns again. This serves two functions

   a. It ensures that the first key detection was not an erroneous one due to a spike noise and
   b. The 20ms delay prevents the same key press from being interpreted as a multiple key press. If after 20 ms delay the key is still pressed, it goes to the next stage to detect which row it belongs to; otherwise, it goes back in to the loop to detect a read key press.

3. To detect which row the key press belongs to, it grounds one row at a time reading the column search time. If it finds that all columns are high this means that the key press does not belongs to the row, therefore it grounds the next row and continues until it finds the row key press belongs to, it sets up the starting address for the look up table holding the scan codes for that row and goes to the next stage to identify the key.

4. To identify the key press, it rotates the column bits one bit at a time in to the carry flag and check to see if it is low. Upon finding the zero, it pulls out the (ASCII code) character for that key from the look up table

VIII. AT24C08

The AT24C08 provides 1024/2048/4096/8192/16384 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 128/256/512/1024/2048 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The AT24C01A/02/04/08/16 is available in space-saving 8-pin PDIP, 8-lead JEDEC SOIC, 8-lead MAP and 8-lead TSSOP packages and is accessed via a 2-wire serial interface. In addition, the entire family is available in 2.7V (2.7V to 5.5V) and 1.8V (1.8V to 5.5V) versions.

Internally organized with 64 pages of 16 bytes each, the 8K requires a 10-bit data word address for random word addressing. The specifications are

The Operating Temperature...**-55ºC to +125ºC**

Storage Temperature...**-65ºC to +150ºC**

Voltage on Any Pin with Respect to Ground…**-1.0V to +7.0V**

Maximum Operating Voltage... **6.25V**

DC output Current… **5.0mA**

SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Data Validity timing diagram).**:** A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Definition timing diagram). A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to Start and Stop Definition timing diagram). The AT24C01A/02/04/08/16 features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations. After an interruption in protocol, power loss or system reset, any 2- wire part can be reset by following these steps:

1. Clock up to 9 cycles.
2. Look for SDA high in each cycle while SCL is high.
3. Create a start condition.

IX. L293D

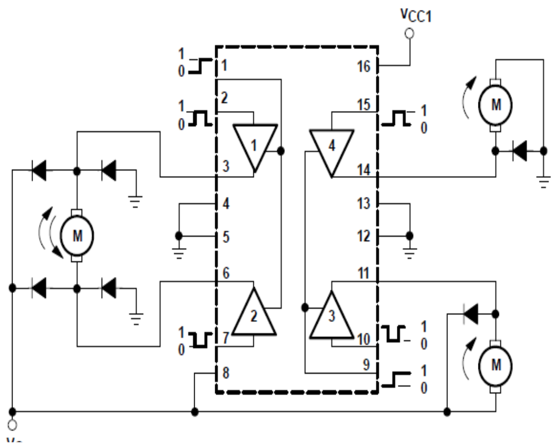

Fig. 8 Block diagram of L293D

The Device is a monolithic integrated high voltage, high current four channel driver designed to accept standard DTL or TTL logic levels and drive inductive loads (such as relays solenoids, DC and stepping motors) and switching power transistors. To simplify use as two bridges each pair of channels is equipped with an enable input. A separate supply input is provided for the logic, allowing operation at a lower voltage and internal clamp diodes are included. This device is suitable for use in switching applications at frequencies up to 5 kHz. The L293D is assembled in a 16-lead plastic package which has 4 center pins connected together and used for heat sinking. The L293D has the following features:

a. 600ma output current capability per channel
b. 1.2a peak output current (non repetitive) per channel
c. Enable facility
d. Over temperature protection
e. Wide Supply-Voltage Range: 4.5 V to 36 V
f. Internal ESD Protection
g. Thermal Shutdown
h. High-Noise-Immunity Inputs
i. Output Current 1 A Per Channel (600 mA for L293D)
j. Peak Output Current 2 A Per Channel (1.2 A for L293D)
k. Output Clamp Diodes for Inductive Transient Suppression (L293D)

X. **RESULTS**

This report will explain about how the utilization of the RFID at tollgates. This is shown in the below diagram device.

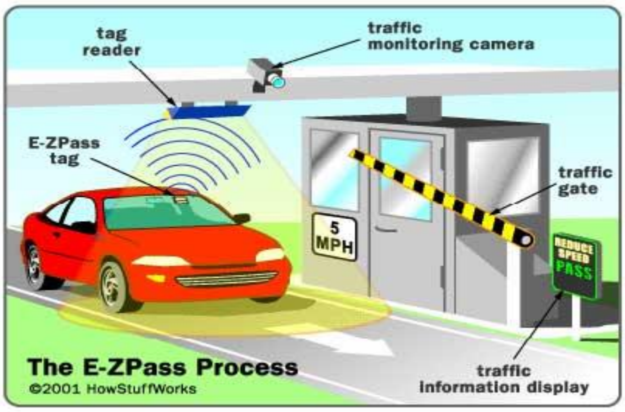

Fig. 9 Toll-Gate Process

The below circuit diagram will explain the above process. Whenever the vehicle enters the toll-gate, the RFID reader will receive the EM waves from the RFID transponder. It will check whether the RFID tag is valid or not. If the card is valid, enter the password using keypad. After that it will allow the vehicle to move and reduce the toll tax from his/her account automatically. If the card is not valid or the password is wrong, alert will come from the buzzer. Depending upon the above process, the message will go to the vehicle owner. This process will allow speed from 50 to 60 kmph. In future, we can extend the speed from 100 to 120 kmph.

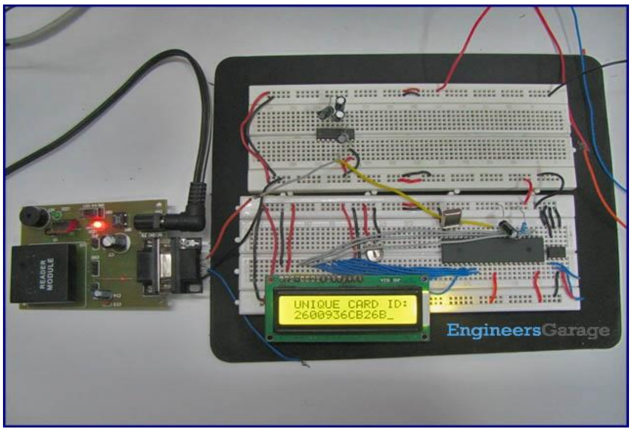

Fig. 10 Circuit diagram

CONCLUSION

This report describes that this system is fully automated and reduces the human error which brings a great evolution in the method of toll system by its flexibility and its fully an authenticated.

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