JOURNAL OF CRITICAL REVIEWS

ISSN- 2394-5125 VOL 5, ISSUE 07, 2018

Utilizing Pulse-Shrinking Fine Stage With Built-In Coarse Gain Calibration Of A 16-piece 2.0-ps Resolution Two-Step TDC in 0.18-µm CMOS

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Abstract

This paper proposes an opportunity to-computerized converter (TDC) that accomplishes wide information range and fine time goals simultaneously. The proposed TDC uses beat contracting (PS) plot in the second stage for a fine goals and two-advance (TS) engineering for a wide range. The proposed PS TDC forestalls an unwanted non uniform contracting rate issue in the traditional PS TDCs by using an implicit counterbalance beat and a balance beat width recognition plans. With a few strategies, incorporating an implicit coarse increase adjustment system, the proposed TS design conquers a nonlinearity because of the sign spread and addition befuddle among coarse and fine stages. The reproduction consequences of the TDC actualized in a 0.18-µm standard CMOS innovation show 2.0-ps goals and 16-piece go that compares to 130-ns input time interim with 0.08-mm2 region. It works at 3.3 MS/s with 18.0 mW from 1.8-V supply and accomplishes 1.44-ps single-shot accuracy.

index Terms—Built-in alignment, beat contracting (PS), time-to-advanced transformation, two stage (TS).**I.**

INTRODUCTION

BASED on the recent progress in CMOS process scaling, time resolution is becoming more and more superior to voltage resolution due to the high-speed transistors and the reduced supply voltage [1], [2]. Recently, a time-to-digital converter (TDC) has been used for various applications, e.g., ADPLLs, space science instruments, jitter measurements, and so on. In particular, with the recent improvement in TDC performance, it is often used in high-precision time-of-flight

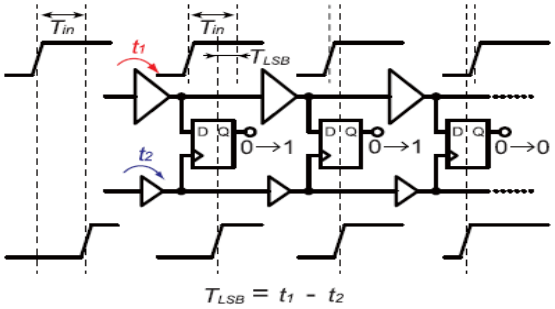


Fig. 1. Simplified schematic of a typical Vernier TDC.

Measurement applications, such as laser range finder [3] and mass spectrometry [4]. It is also used in fluorescence lifetime imaging applications [5]. In these applications, which are the main target applications of this paper, fine time resolution and wide dynamic range are demanded at the same time [6]. Since the TDC determines the overall performance of the measurement, a few ps time resolution with low jitter at a sampling rate of several MS/s is often requested. In terms of fine resolution, several time conversion techniques that realize sub-gate-delay resolution have been proposed. A Vernier TDC is widely adopted, thanks to the simplicity of its design concept [6]–[9]. As illustrated in Fig. 1, a typical Vernier TDC needs two independent delay lines that are often implemented as ring delay lines to save area. Two lines have different delay steps, e.g., $t1$ and $t2$ ($t2 < t1$), and thus, the initial time interval Tin between two rising transitions gradually shrinks until the moment when the transition in lower delay line catches up with that in the upper one. By tuning the delay difference TLSB = $t1-t2$, we can realize fine time resolution. However, this architecture requires two independent delay lines, where mismatch between them is inevitable. On the other hand, a pulse-shrinking (PS) TDC shown in Fig. 2, which is also a type of Vernier TDCs, utilizes the delay difference between rising and falling transitions of a buffer instead of the two independent delay lines [10], [11].

The buffer is intentionally designed to have different rise and fall delays, e.g., t_r and t_f ($t_f < t_r$), and thus,

ISSN- 2394-5125 VOL 5, ISSUE 07, 2018

the incoming pulse width shrinks $T_{LSB} = t_r - t_f$ by propagating through each buffer stage until it disappears. Unlike Vernier TDCs,

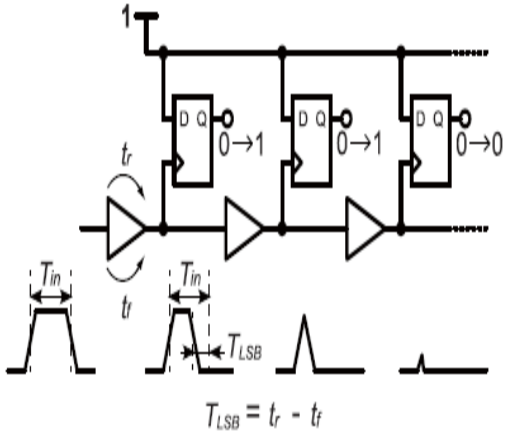


Fig. 2. Simplified schematic of a typical PS TDC.

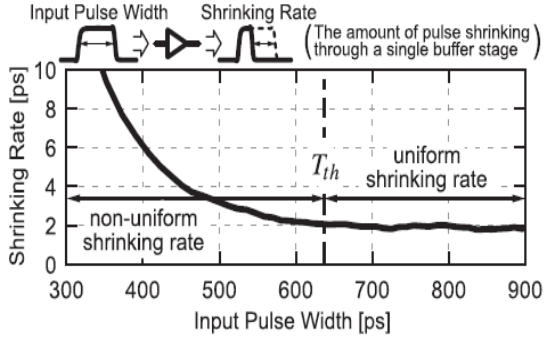


Fig. 3. Simulated PS rate versus input pulsewidth.

The architecture of the TDCs discussed so far focused on fine time resolution. However, for a wide dynamic range,

it may become unattractive. For example, a Vernier TDC that has an N-bit and time resolution uses 2N delay elements and has × 2N dynamic range. If the time resolution is reduced by half, the dynamic range is also halved. Then, to keep the same dynamic range, the TDC requires additional 2N delay elements that increase area occupation, slow down conversion rate, and increase jitter accumulation as N becomes larger. A looped TDC architecture is one of the simplest ideas to extend the dynamic range while preventing area increase [13]. A loop counter determines how many times the start signal rotates on the loop until the stop signal catches up. The overall conversion result can be calculated from the counter output and the thermometer code provided by the DFFs. In an ideal situation the input range can be

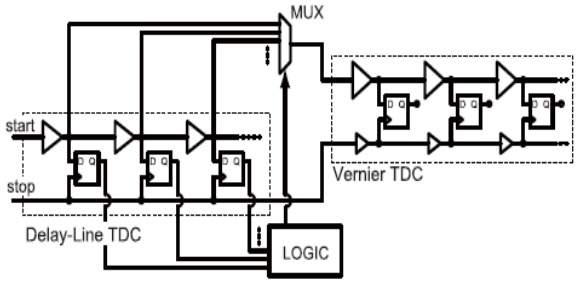


Fig. 4. Schematic of a typical TS TDC [14], [15].

In this paper, in order to achieve a fine resolution and wide range at the same time, we employ a sub-gate-delay resolution PS architecture as the fine TDC of the TS architecture and propose several techniques to overcome the issues in the conventional PS and TS TDCs discussed so far. The proposed PS TDC incorporates a novel pulse injection with a built-in offset pulse and always keeps the propagating pulse wider than the offset one. Then, the PS TDC finishes the conversion process when it detects the original offset pulse width that is set wider than the threshold Tth to avoid the non uniform PS rate issue, as shown in Fig. 3 [11]. Based on this scheme, the PS TDC realizes a fine time resolution, avoids unneeded jitter accumulation, and saves conversion time and power consumption, while it inherits the advantages of the conventional PS TDC architecture. The proposed TS TDC avoids the use of the inter-stage multiplexer and overcomes the resolution mismatch issue with a built-in coarse gain calibration mechanism so that the proposed TS TDC realizes a wide dynamic range and a fine time resolution at the same time.

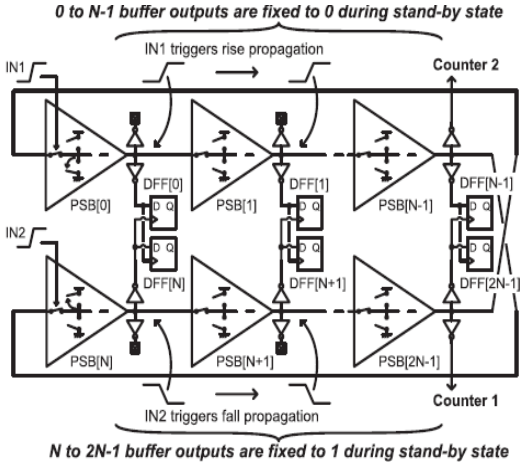


Fig. 5. Block diagram of the proposed fine TDC based on the PSBR.

ISSN- 2394-5125 VOL 5, ISSUE 07, 2018

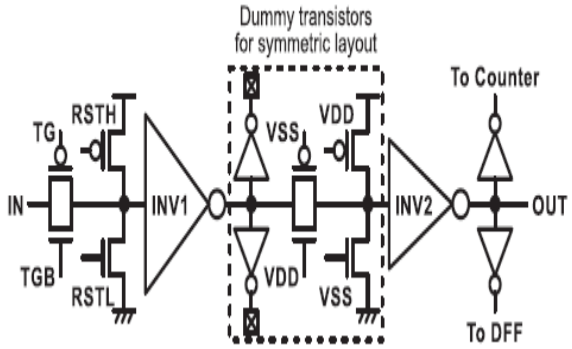


Fig. 6. Detailed schematic of the PSB.

The rest of this paper is organized as follows. In Section II, the architecture and conversion principle of the proposed TDC are described. Section III presents the circuit implementation and post-layout simulation results of the proposed TDC. Then, Section IV concludes this paper.

II. PROPOSED TWO-STEP TDC ARCHITECTURE

A. Pulse-Shrinking Fine-Stage TDC

The block diagram of the fine-stage TDC based on PS buffer ring (PSBR) is illustrated in Fig. 5. It is mainly composed of 2N-stage PS buffers (PSBs). The output of kth PSB (k = 0, . . . , N − 1) is connected to both a data input of kth DFF and a clock input of (N + k)th DFF, while the output of (N + k)th PSB on the opposite side of the ring is connected to both a data of (N +k)th and a clock of kth DFFs. Besides, the outputs of (N−1)th and (2N−1)th PSBs are connected to counters outside the PSBR core

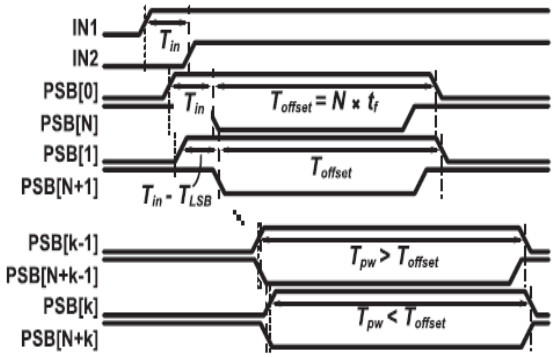


Fig. 7. Timing diagram of the PS TDC.

Since the output of the PSB at the opposite side of the ring is supposed to have a signal transition of an opposite
polarity when the propagating pulse width T pw becomes equal to the original built-in offset pulse width T offset, the kth PSB output rises later than the falling edge of the (N + k)th PSB output, thus the kth DFF alters its output from 0 to 1, as illustrated in Fig. 8. By identifying this DFF output transition, this TDC detects the original built-in Toffset and triggers the completion signal. Therefore, even if T offset fluctuates due to process variation, the absolute value of Toffset has no impact on the conversion process. Since T offset is chosen by design to satisfy Toffset > Tth in Fig. 3, the proposed TDC does not suffer from the non uniform shrinking rate issue.

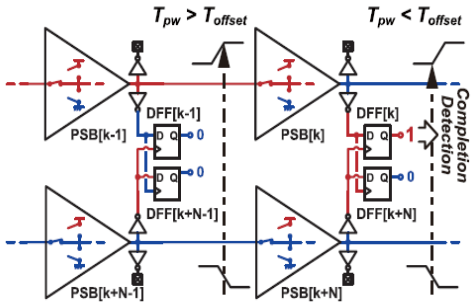


Fig. 8. Detailed PSBR schematic at the moment of the completion of conversion.

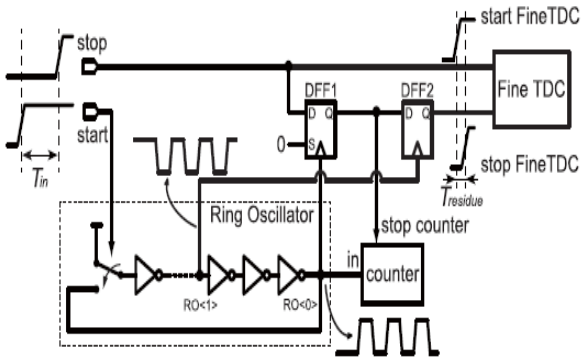


Fig. 9. Block diagram of the proposed TS TDC.

B. Architecture of the Two-Step TDC

The block diagram of the proposed TS TDC architecture is illustrated in Fig. 9. A ring oscillator with a counter
works as the coarse TDC, and the PS TDC in Section II-A works as the fine stage. In the proposed TDC, the two TDCs are coupled through two DFFs unlike the conventional TS TDCs to avoid the non idealities

ISSN- 2394-5125 VOL 5, ISSUE 07, 2018

of the inter-stage multiplexers. Though the second DFF, DFF2 in Fig. 9, connected to the fine TDC seems to be redundant, it alleviates a metastability issue in DFF1 due to asynchronous timing between RO0 and the input stop signal. Moreover, the two DFFs have another role for the proposed built-in calibration mechanism, which is mentioned in Section II-C

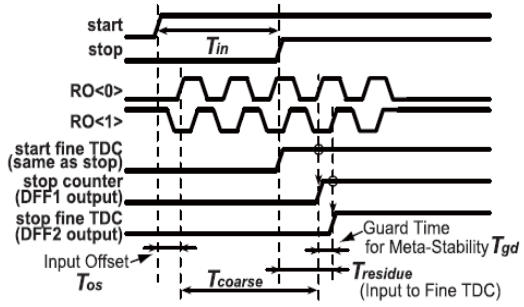


Fig. 10. Timing diagram of the proposed TS TDC.

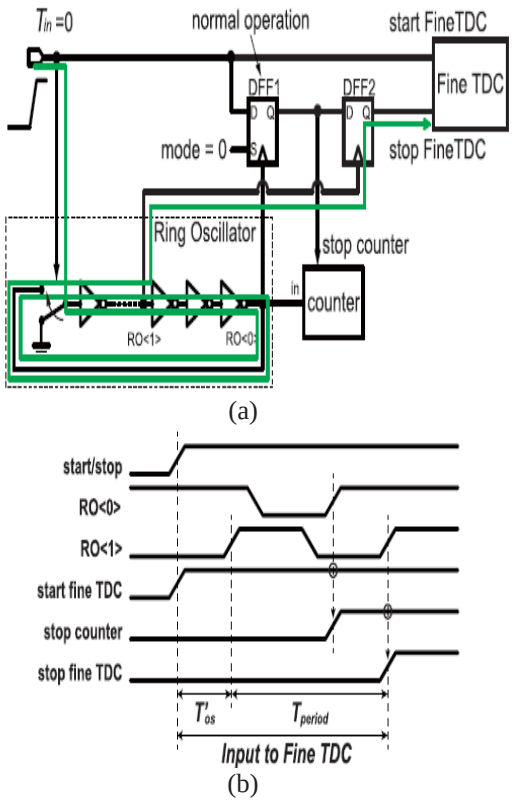
works as guard time to suppress the metastability. Through the above-mentioned procedure, the time residue caused by this roundup, $T_{residue}$, in Fig. 10, is injected into the second stage TDC for a fine conversion. Eventually, the overall input time interval is resolved according to

$$T_{in} = T_{os} + T_{coarse} + T_{gd} - T_{residue}$$

C. Built-In Coarse Gain Calibration

The proposed calibration scheme is based on the built-in measurement mechanism. The required ratio of the resolutions can be obtained by measuring a time interval that corresponds to the 1 LSB of the coarse TDC with the fine TDC. In the calibration process, two different paths are switched by utilizing S (Set) input of DFF1 that is used to fix its output Q to high, as illustrated in Figs. 11 and 12. First of all, during the calibration mode, the input of the first-stage inverter is fixed to GND before the process starts. When DFF1 is in normal operation with 0 input to the S-port, as illustrated in Fig. 11(a), given Tin = 0, the fine TDC is stopped after one period of coarse oscillation Tperiod plus the input offset time T

os, as summarized by the timing diagram



PROTOTYPE IMPLEMENTATION AND SIMULATION

The proposed TS TDC is implemented in a 0.18-μm standard CMOS technology, as shown in Fig. 13, and its
performance is verified with post-layout simulation.

A. Fine-Stage TDC

The lower part of Fig. 13 shows PSB placement of the PSBR core in the fine TDC, which has 32 PSB stages. kth
and (k + 16)th PSBs (k = 0, . . . , 15) are laid next to each other to relax DFF connections shown in Fig. 5, and PSBs are arranged so that the wire lengths of inter-PSB connections are equal. The transistor size and the current consumption of the inverters in PSB have to be carefully chosen because the impact of jitter accumulation and process variation needs to be considered. We determined the transistor sizes of the PSB based on the jitter analysis in eq

ISSN- 2394-5125 VOL 5, ISSUE 07, 2018

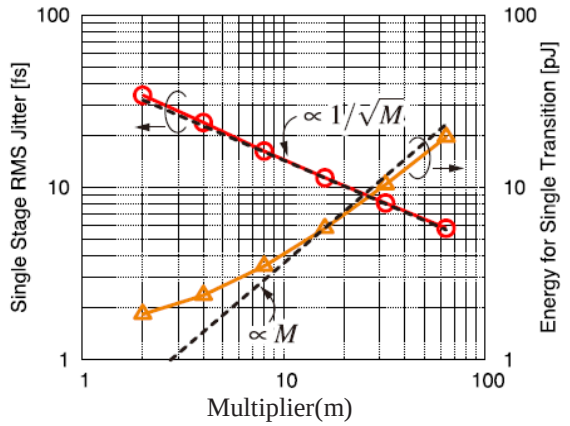


Fig. 14. Schematic-level simulation results of jitter and energy of a singlestage PSB for a single rise transition depending on the transistor width. For INV1 in PSB, WpMOS = 8.32 × M µm and WnMOS = 4.00 × M µm. For INV2, WpMOS = 8.00× M µm and WnMOS = 4.00× M µm. The rms jitter is calculated with 1024 times Monte Carlo simulations with thermal noise. the initial noise on the output capacitor [17], the jitter due to the white noise caused by channel resistance is given by

$$\sigma_{t_{dP}} \approx \sqrt{\frac{4kT\gamma_P t_{dP}}{I_P(V_{DD} - V_{tP})}} \qquad (3)$$

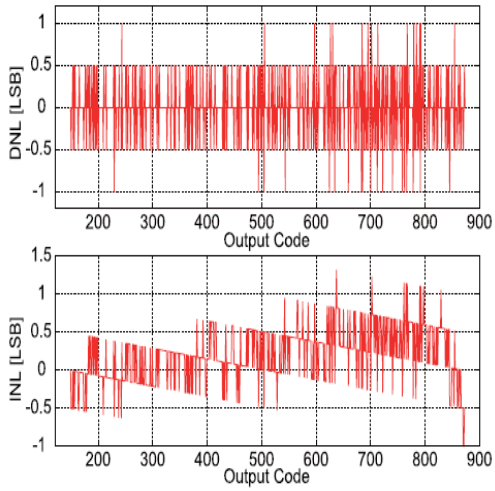


Fig. 16. Simulation results of DNL and INL of the fine-stage PS TDC.

B. Two-Step TDC

The transistor sizes of the ring oscillator in the coarse TDC, which has 15 stages of inverters, are also determined based on the jitter analysis in [17]. As shown in Fig. 17, for the coarse stage ring oscillator, we have verified the trends of jitter and energy for a single rise transition with schematic-level simulation by sweeping the transistor width. The black dashed lines are normalized with the simulation results at M = 16. As expected, the jitter and energy are clearly in proportion to 1/ M and M, respectively, because the coarse stage ring oscillator uses simple inverters. Since, in our TS TDC, the coarse stage covers up to 7-bit range, with the maximum

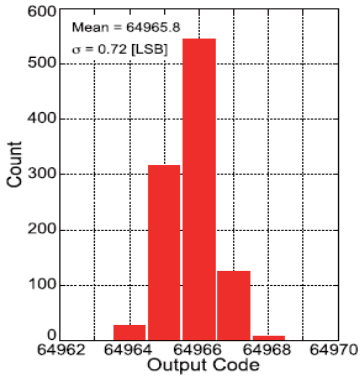


Fig. . Post-layout simulation result of single-shot code distribution of the TS TDC.

Finish the conversion. In this case, 47.8% of the total power is consumed in the fine stage, while the rest is in the coarse stage. Simulated DNL and INL are plotted in Fig. 19. The range of the simulation is at the middle of the input time interval range, where the INL becomes its maximum because the transfer characteristic of the TDC has slightly arcuate shape caused by the calibration error. The detailed transfer characteristic of this range is also shown in Fig. 18. The TDC achieves the maximum DNL and INL of −1.0/+1.0 and −2.0/+1.0 LSB, respectively.

Ref.	TCAS'14 [6]	JSSC'10 [7]	MEJ'15 [9]	JSSC'12 [18]	JSSC'13 [19]	JSSC'14 [20]	ASSCC'16 [11]	This work
Architecture	3D Vernier	2D Vernier	Vernier Sub-Ranging	Cyclic	Two-Step (Time Amp.)	Pipeline	Pulse Shrinking (PS)	Two-Step PS
Tech. [nm] (Meas./Sim.)	130 Meas.	65 Meas.	130 Meas.	130 Meas.	65 Meas.	65 Meas.	180 Meas.	180 Sim.**
Resol. [ps]	7	4.8	5	1.25	3.75	1.12	1.8	2.00
Precision rms [ps] (T_{in} at the meas. or sim.)	20.8 (@1.4 ns)	-	2.05 (0~300 ps)	~1.25* (@40 ps)	-	0.77 (@~348 ps*)	2.16 (@860 ps)	1.44 (@129.5 ns)
Rate [MS/s]	25	50	20	50	200	250	4.4	3.3
Range [bit]	11	7	6	8	7	9	9	16
DNL [LSB]	0.8	1	0.63	0.7	0.9	0.6	1.2	1.5
INL [LSB]	1.5	3.3	1.47	3.0	2.3	1.7	8.7	4.2
Power [mW]	0.33(@1MHz)	1.7	1.15	4.3	3.6	15.4	3.4	18.0
Area [mm^2]	0.28	0.02	0.7	0.07	0.02	0.14	0.07	0.08
FoM [pJ/conv.-step]	0.40	1.14	1.96	1.34	0.46	0.32	14.6	0.43

* calculated from the figure of the measurement result. ** Monte-Carlo simulation result that leads to the worst FoM.

ISSN- 2394-5125 VOL 5, ISSUE 07, 2018

The performance of the proposed TS TDC is compared with several recently reported sub-gate-delay resolution TDCs in Table I. To make a fair comparison, the figure of merit (FoM), which is widely used for TDC comparison,
is adopted [6], [19], [20]. The FoM is defined as

$$\text{FoM} = \frac{\text{Power}}{(2^{N_{\text{linear}}} \times f_s)}$$

where the effective number of linear bits (*N*linear) is given by

$$N_{\text{linear}} = \text{Range [bit]} - \log_2(\text{INL} +$$

The Monte Carlo simulation results with the worst Fo M case are listed for the proposed TDC. The proposed TDC realizes ultra wide range and fine time resolution at the same time while achieving competitive FoM using mature 0.18-µm CMOS technology.

IV. CONCLUSION

This paper presented a wide input range and fine-time resolution TDC that combines PS and TS architectures.
In the fine-stage PS TDC, an undesirable non uniformity of pulse shrinking rate in the conventional PS TDCs is avoided by a novel pulse injection with a built-in offset pulse and an offset pulse width detection schemes. This contributes to fine resolution and low-jitter time-to-digital conversion, while it inherits the advantages of the PS TDC architecture, such as small-area implementation. The proposed TS architecture is applied to the PS TDC in order to expand the input range. The proposed TS TDC that incorporates a built-in coarse gain calibration mechanism overcomes the practical difficulty due to the non ideality of the inter-stage signal propagation path and the gain mismatch between the two stages. The detailed simulation results demonstrated that the proposed TDC realizes 16-bit wide dynamic range and 2.0-ps fine resolution at the same time. It achieves a competitive FoM
using mature 0.18-µm technology in comparison with the recently reported sub-gate-delay resolution TDCs.

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ISSN- 2394-5125 VOL 5, ISSUE 07, 2018

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