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PSPWM BASED SCMLI TOPOLOGY WITH A REDUCED NUMBER OF SWITCHES FOR AC POWER DISTRIBUTION SYSTEM

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Abstract:

Creating a Phase Shift Pulse Width Modulated (PS-PWM) Switched Capacitor Multi Level Inverter was the primary motivation for this study (SCMLI). Input voltage and current waveforms from multiple photovoltaic (PV) sources are transformed into usable electrical power by power electronics converters. High-frequency alternating current (AC) electricity from solar photovoltaics (PV) is growing in popularity. By reducing the number of stages and components often used in power conversion, DC/AC SCMLIs, for example, may increase the speed of power conversion. We present a new PSPWM-based SCMLI layout, which requires fewer switches and a voltage balance across the floating capacitor than conventional designs (FC). There is one primary dc source and two auxiliary dc sources in the proposed topology. In theory, the proposed architecture might provide a voltage output (Vo) that is twice as large as the input voltage. Compared to the previous topologies, it has a greater discharge rate. Decreases in load voltage reduce the voltage stress experienced by switches. The proposed simulation results are analysed in MATLAB/SIMULINK.

Keywords: Power factor correction, Pulse width modulation, a stepped-up inverter, a float-charge capacitor, and ac-power-distribution frequencies

INTRODUCTION

The ever-increasing need for energy, as well as the apparently endless possibilities of solar power, may both be contributing factors to the rapid expansion of PV-fed applications. The development of power electronics will make photovoltaics more practical for application in settings that previously required less efficient power converters. High-frequency power distribution systems, such as those used in aerospace, communications, and computer applications [1, 2], benefit greatly from the integration of PV with power electronics technology. Using high-frequency alternating current is essential for an airplane's electrical system, as seen in the diagram to the right. Multilayer inverters (MLIs) are one kind of PV power converter, and they are used in the vast majority of commercial and industrial PV systems. The MLI's low dv/dt ratio and harmonic distortion are two of its many advantages (THD). In addition to AC drives, FACTS devices, renewable energy, and microgrids, it is clear that MLI has a wide variety of other potential uses. The term "multilevel inverters" is used to describe a broad category that includes many different types of topologies (MLI). High-voltage and high-power applications are where standard topologies really shine [3]. Although these topologies make extensive use of switches, diodes, and dc-link capacitors/dc sources, they only experience mild dv/dt stress. In [4], we see the introduction of a new MLI architecture that is both more efficient and gentler on the various components of the system. In these settings, the dv/dt pressure rises, but the number of switches in use drops. To lessen the workload and number of switches, [5-15] also includes SCMLIs. When a high voltage level has to be created with a minimal number of switches, SCMLI topologies are the way to go. These configurations use just a single dc supply and experience little dv/dt stress. The FC's

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utilisation is determined by the range of input voltages.

The cascading design makes it possible to explore the hierarchical structure of the company in more depth. It generates twice as much energy as it consumes. To further lessen the stress on the switches and the voltage they are exposed to, new SCMLI topologies with a voltage gain of 1:2 are advised for 9L in [11-13]. The voltage waveform output is limited to 9L in both topologies, thus if you need more power, the cascaded topology is your best bet. Because of this, the SCMLI architecture for the 13L inverter was initially shown in [14-18]. Simple device with voltage gain of 1:2 is used in [14] to generate a 13L from two DC sources; cascaded design is again recommended for higher voltages. These architectures need more switches and FCs, precisely as the topologies in [15–18]. In [15], we have a diagram of a cross-shaped design that can boost voltage while keeping it stable. Electricity exerts a great deal of force on the switch, which is made up of many separate parts. Six Vines may be obtained using 13L-SCMLI [16], which is a lot. There are a total of thirteen switches, two diodes, and three FCs utilised in this network topology. See [17, 18] for examples of the dual-power supply 13L inverter. It has risen in size, but the output voltage has increased by a factor of six. In the same vein as [18], just using a single dc source is not feasible. The new 'K' type generalised SCMLI design in [19] has a reduced power component despite a voltage rise of 1.5 vin with more components.

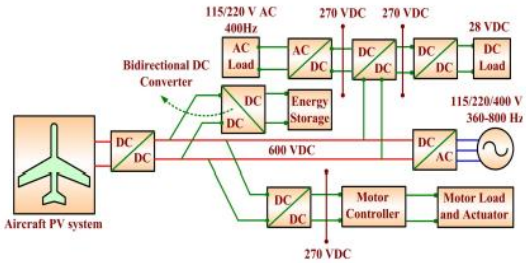

Fig. 1. Typical aircraft electric system without auxiliary source.

For the proposed design, either a single dc source with dc-link capacitors or three dc sources linked in series are viable options for the power supply. Several advantages of multi-source MLIs are shown in [20], and many of them need fewer switches. The source-side cell, which may establish connections between the sources in a wide variety of ways, generates multilevel output at the first stage. With some tweaks, this design might be used with a broader spectrum of voltage sources by permitting the creation of more voltage levels with fewer components. If the design can produce numerous voltage levels with fewer parts, it might be scaled up to handle multiple voltage sources. The output voltage is utilised to stress the switches, which is a fundamental drawback of such designs. In order to mitigate these problems, this study introduces a unique 13L-SCMLI design by reducing the overall number of switches and the stress exerted on the switches by voltage. A dc source's FC number specifies the range of voltages it may provide. A longer charging period than a shorter discharging time is also beneficial to the FC's performance. Advantages abound, and the planned implementation of I Topology is among them. To recap, (I) has a charging time greater than a discharging time and a dv/dt stress equal to Vin, (ii) generates the 13L output voltage level from a single dc source and fewer switches, (iii) is capable of self-voltage balancing and two times boosting, and (iv) uses a single FC. Because of this, the front-end dc/dc converter's maximum input voltage has dropped. Pulses for switching are generated using Nearest Level Modulation (NLM). Its benefits include low switching loss and simple digital controller integration. In most cases, as seen in [22], a standard NLM will choose the output value that is most similar to the reference voltage. The dc-offset is set to 0.25 in Enhanced Nearest Level Control. That causes an increase in the RMS value as well. When the input voltage range is narrower, the voltage THD increases. According to [24], if you use a dc-offset of 0.40, your maximum loss will be 0.4Vin. This is well below the threshold at which dc losses become noticeable.

II. PROPOSED 13 LEVELS INVERTER CONFIGURATION

A. Proposed Circuit

Figure 2 provides a pictorial illustration of the 13L-SCMLI that has been suggested. Voltage across the FC equals Vin minus VFC if V1, V2, and V3 are all constant DC voltages. The bidirectional

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switches Sab and Sab' both employ diodes, however Sab uses four while Sab' uses two IGBTs in anti-series with parallel diodes. With respect to Figure 2(a), all three DC-link capacitors are linked to the aforementioned three DC sources (b). In order to avoid creating a short circuit, the SR (on), SSR (on), SSR' (on), and SSR' (on) switches should not be turned on at the same time. There is a cross-connection between all of the switching capacitor parts in this particular cell.

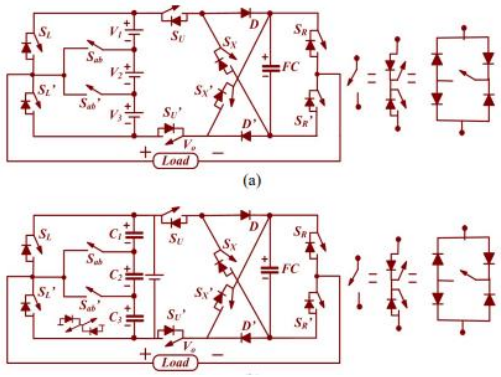

Fig. 2. Circuit schematic of a high-frequency 13L inverter with either (a) numerous dc inputs or (b) a single dc input.

B. Switching pattern and modes of operation

The switch shown in Table I's Figure 3 can be set up in a variety of ways. Figure 2(a) provides a schematic of how 13L functions, while the other two figures convey the same information in different ways. Figure 3 illustrates the constituent parts of these zones:

TABLE I. Switching pattern for proposed 13-level MLI

State	ON State Switches	DC Source		FC*	V_O
		Fig.2 (a)	Fig.2 (b)		
A	S_{ab}, S_U, D, S_R, S_U', D'	V_1	C_1	C	$+V_{in}$
B	S_{ab}', S_U, D S_R, S_U', D'	V_1+V_2	C_1+C_2	C	$+2V_{in}$
C	S_L', S_U, D, S_R, S_U', D'	$V_1+V_2+V_3$	$C_1+C_2+C_3$	C	$+3V_{in}$
D	S_{ab}, S_U, S_R, S_X	V_1	C_1	D	$V_{in}+V_{FC}$
E	S_{ab}', S_U, S_R, S_X	V_1+V_2	C_1+C_2	D	$2V_{in}+V_{FC}$
F	S_L', S_U, S_R, S_X	$V_1+V_2+V_3$	$C_1+C_2+C_3$	D	$3V_{in}+V_{FC}$
O	S_L, S_U, S_X, S_R' S_L', S_U', S_X', S_R	-	-	-	$0V_{in}$
A'	S_{ab}', S_U, D, S_R', S_U', D'	V_3	C_3	C	$-V_{in}$
B'	S_{ab}, S_U, D, S_R', S_U', D'	V_2+V_3	C_2+C_3	C	$-2V_{in}$
C'	S_L, S_U, D, S_R', S_U', D'	$V_1+V_2+V_3$	$C_1+C_2+C_3$	C	$-3V_{in}$
D'	S_{ab}', S_X', S_R', S_U'	V_3	C_3	D	$-V_{in}-V_{FC}$
E'	S_{ab}, S_X', S_R', S_U'	V_2+V_3	C_2+C_3	D	$-2V_{in}-V_{FC}$
F'	S_L, S_X', S_R', S_U'	$V_1+V_2+V_3$	$C_1+C_2+C_3$	D	$-3V_{in}-V_{FC}$

*State of FC, C-charging of FC, D-discharging of FC

In state A, the three dc power sources are connected in series with the FC through switches D, SU', and D', charging it from 0 V to 3 Vin. By combining SR and Sab switches, we can generate V1 (Vin) for the whole load.

State B requires the identical set of switches as State A (SU, D, SU', and D') with Sab disabled in order to maintain the FC voltage (VFC) at 3 Vin. The voltage across the load is calculated by multiplying the outputs of the two dc sources, V1 and V2 (plus two Vin).

In the third and final operating condition, the maximum Vin across the load is achieved by adding the minimum DC source voltage to V1 and V2. Presently, the FC owes 3 Vin. It comes with four switches: two load switches (SU, D, SU', and D'), and two charge switches (SU, D, SU', and D'). In the first three, FC charges are standard procedure. The second stage involves charging the FC from two separate dc sources before releasing it.

Switches SU, SR, and SX are turned on to discharge the FC in state D. To calculate the voltage across the load, multiply V1 by VFC and then VFC by Vin.

When the SU, SU's, SR, and SX switches are all enabled, a state known as +2 Vin +VFC is achieved.

To enter State F, you must invert SL', SU, SR, and SX. To calculate the applied voltage, use the equation: Vo=+3Vin+VFC. As a result of the information it receives, the FC is both energised and depleted. Take your pick among the four similar occurrences that have occurred thus far. The FC can only be charged with a power factor of 1 if the SL, SU, D, and SR switches are all on at the same time. There are no extra expenses incurred by the FC as a consequence of a power factor mismatch.

During the FC's inactive half-cycle, state A' is converted to state C', and then the charge is released to state F. Table I lists the stages and the switches that are turned on by them. You can see the switch pulses generated by the NLM technique

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in Fig. 4. Instead of using conventional SPWM, the NLM employs a fundamental frequency approach strategy to reduce switching losses. These changes might occur anywhere from about 360 hertz to around 1 kilohertz. NLM stands for the National Library of Medicine, and its full definition is as follows: Simply dividing the two values (Verve and Vons) will give you the Modulation Index.

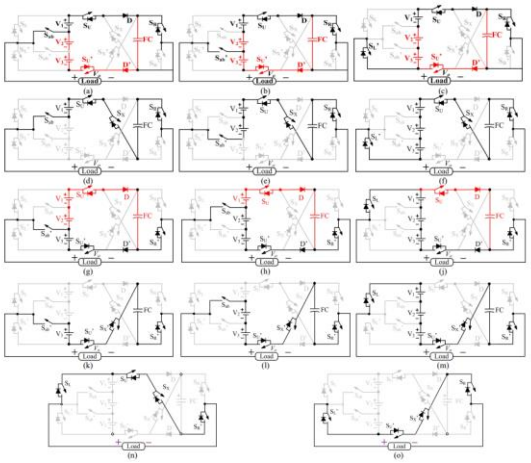

Fig. 3. Here, a–f represent States A–F, g–m represent States A–F, n–o represent State 0, and so on.

The corresponding voltages for the different states are depicted in

III. PROPOSED PSPWM TECHNQUIE

Each triangle carrier in PSPWM oscillates at the same frequency and has the same peak-to-peak amplitude. A phase difference will exist between any two consecutive carrier waves. An information carrier signal with a voltage of (m-1) and a phase shift of =(360°/m-1) is needed for transmission. Producing gate signals involves comparing the carrier wave to the modulating signal.

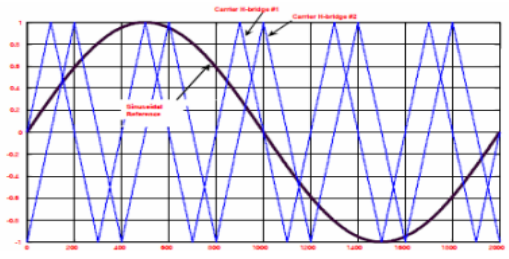

Fig. 4 Phase Shifted Carrier PWM

IV.SIMULATION RESULTS

TABLE 1. Parameters of 13-level MLI

I/P (Vdc)	100V
Load	R=100 Ohm, L=20 MH R=40 Ohm, L=2mH
IGBT	600V, 32A
O/P Freq.	F1=360Hz, F2=400Hz

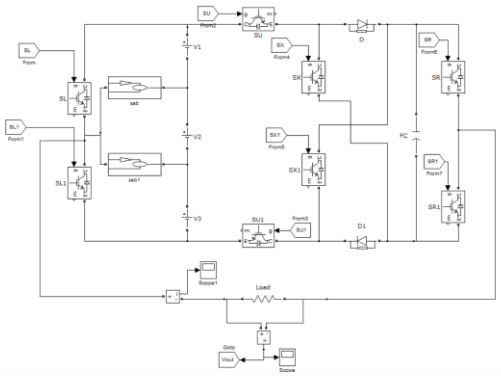

Fig.5 The circuit diagram of the 13-level MLI can be found in MATLAB/SIMULINK.

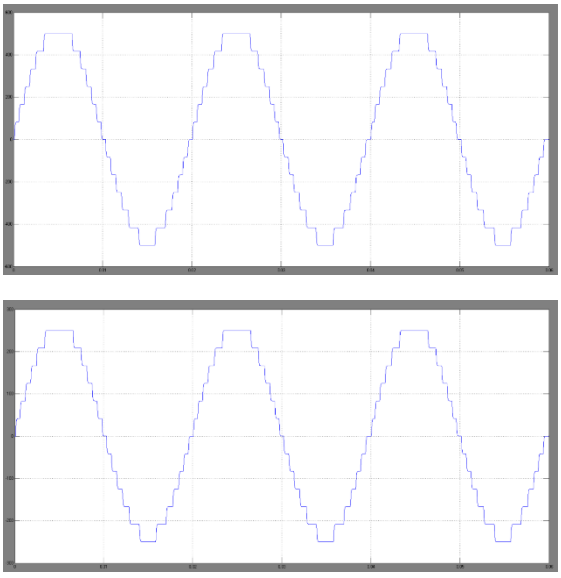

Fig.6 computed value for R = 100, 10 A/div in a simulation

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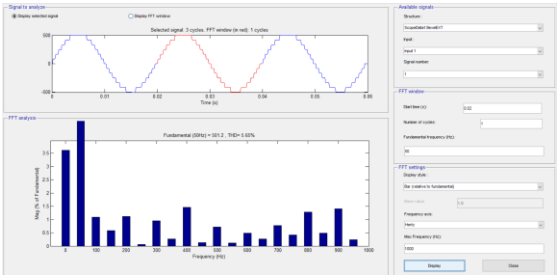
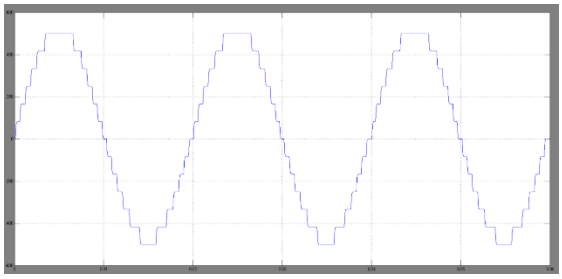


Fig.7 The voltage at the 13th level has a THD of 5.65%.



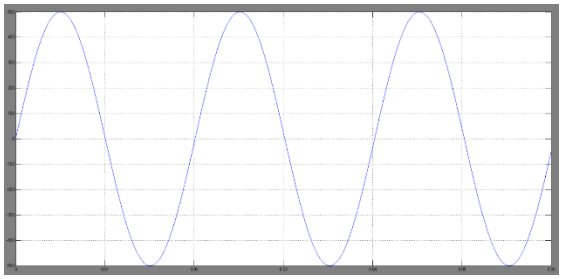


Fig.8 Waveforms of the voltage and current delivered to Load 1 at 360 hertz

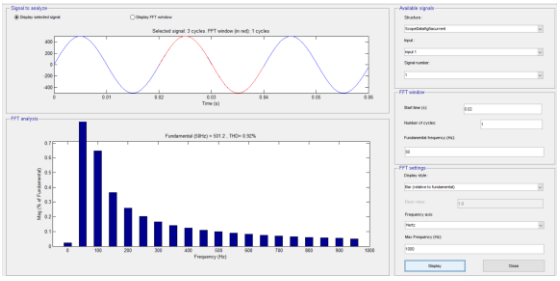
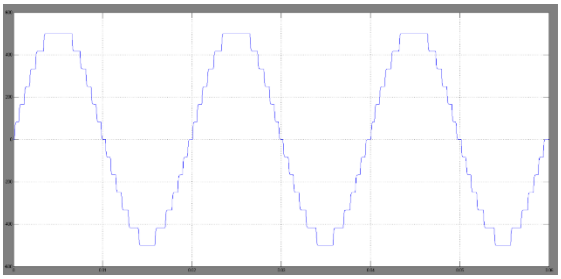


Fig.9 THD (harmonic distortion) at Load 1 and 360 Hz is typically 0.92 percent.



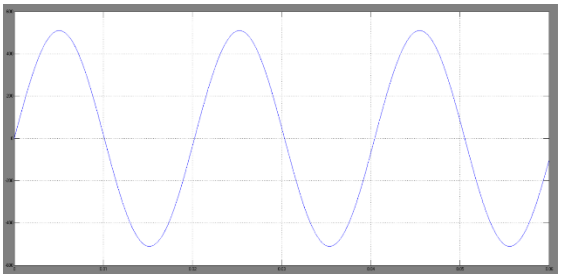


Fig.10 the voltage and current waveforms supplied to Load 2 at a frequency of 360 hertz

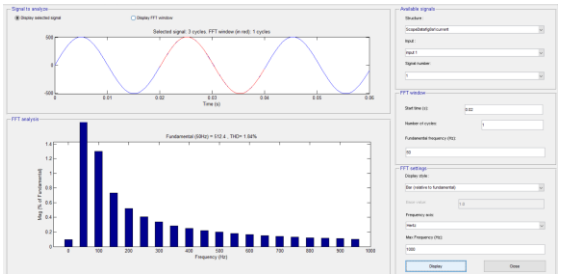
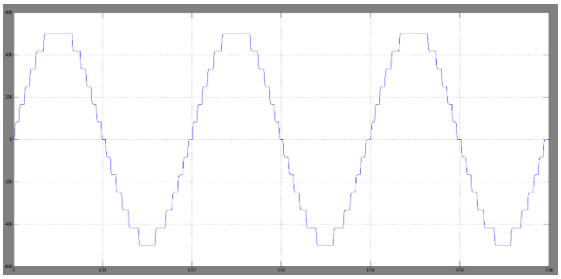


Fig.11 The total harmonic distortion (THD) of the output current at load 2 and 360 Hz was 1.84 percent.



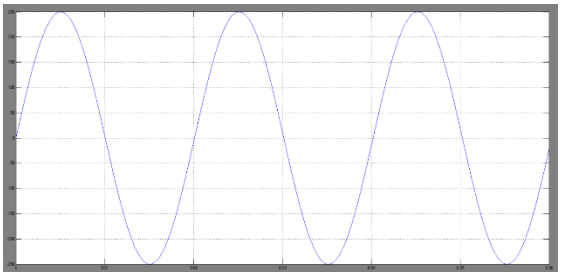


Fig.12 Waveforms of voltage and current output to Load 1 at 400hertz

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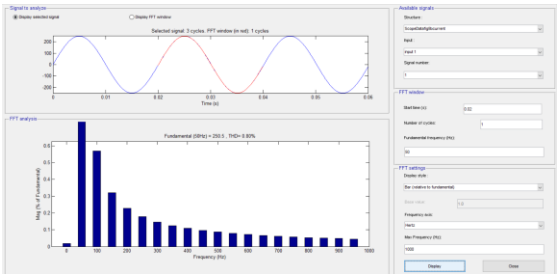


Fig.13 The Total Harmonic Distortion (THD) at 400 Hz under Load 1

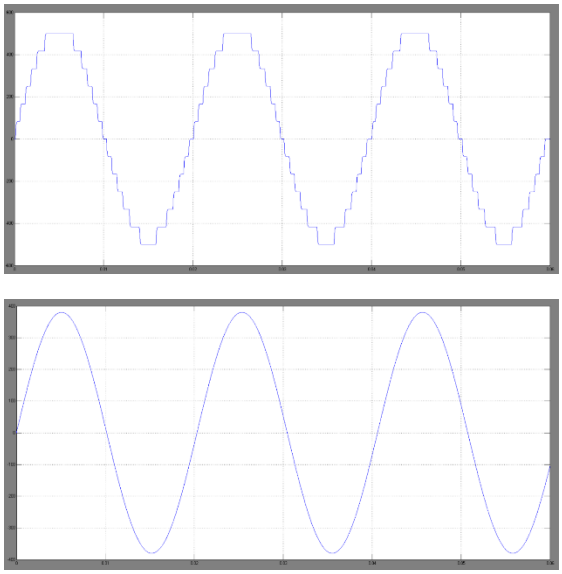


Fig.14 Current and voltage waveforms at Load 2 at 400 Hz are shown below.

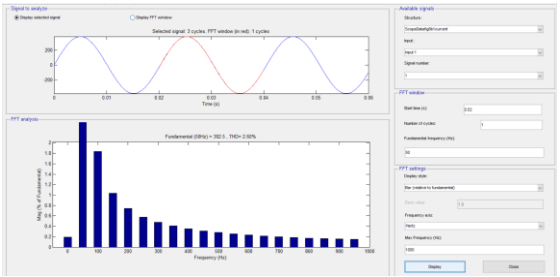


Fig .15 Power supply total harmonic distortion (THD) at load 2 and 400 hertz (2.60%)

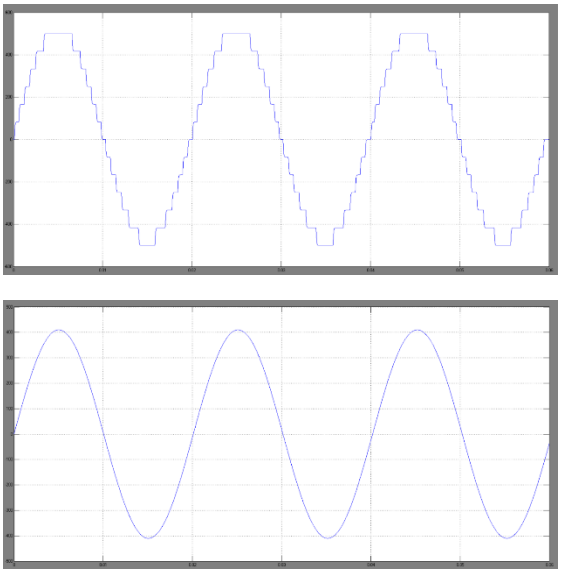


Fig.16 Voltage and current waveforms at 1000 Hz for Load 1.

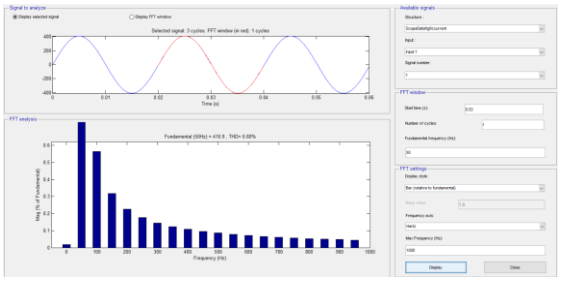
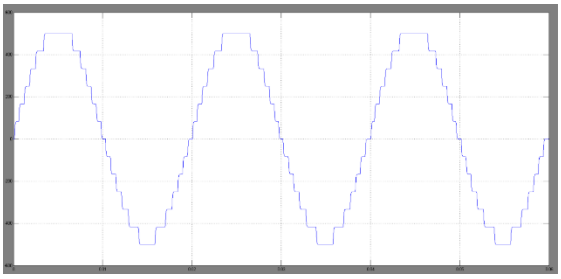


Fig.17 THD (threshold harmonic distortion) at 1000 hertz with load 1.



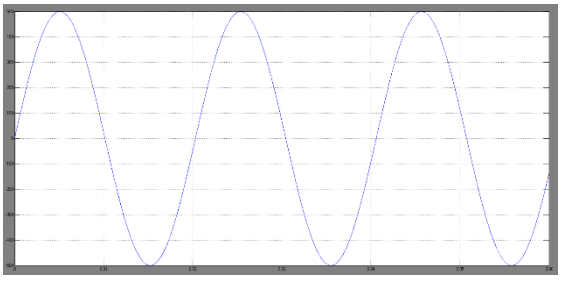


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Fig.18 Voltage and current waveforms at 1000 Hz in Load 2.

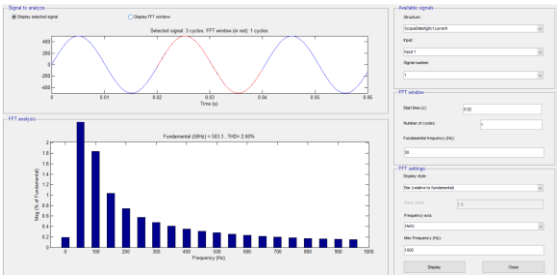

Fig.19 Current distortion at load 2 and 1000 Hz (THD = 2.6)

COMPARISION TABLE

	Existing System (THD%)	Proposed System (THD%)
Output voltage	6.75%	5.65%
Output current (Load1) at 360Hz	1.07%	0.92%
Output current (Load2) at 360Hz	2.06%	1.84%
Output current (Load1) at 400Hz	0.96%	0.80%
Output current (Load2) at 400Hz	2.78%	2.60%
Output current (Load1) at 1000Hz	0.91%	0.80%
Output current (Load2) at 1000Hz	2.74%	2.60%

CONCLUSION

Evidence suggests that the new PSPWM-based 13L-SCMLI design alone is sufficient to raise the voltage. While striving to decrease the overall number of switches, the suggested topology includes a self-balanced FC voltage. The 13L-SCMLI proposal, which uses PSPWM, has been compared to a number of well-known modern architectures. The results show that the proposed 13L-SCMLI topology reduces the total number of switches while significantly improving the number of FCs, voltage gain, and charging/discharging cycles. Unfortunately, not all possible topologies can simultaneously satisfy all of these conditions. We used the experimental setup to test the proposed design at three distinct fundamental frequencies and then performed simulations and analyses on the resulting data. It is evident that the two figures for THD and output power were so close together. Comparing the simulation's performance to that of the experiment, it comes quite close. The simulation findings included a power analysis at each of the three frequencies to take into account fluctuations in the dynamic load. The proposed architecture boasts a 98% efficiency at 600W at unit power factor, making it ideal for high frequency power distribution applications like aviation.

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