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FAULT TOLERANT SRAM ARRAY STRUCTURE FOR RELIABILITY ENHANCEMENT AGAINST FAILURES

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Abstract

Resistive open defects in memory are gaining higher attention to the growing technology. With the advanced deep submicron technology, effects of change in temperature, supply voltage and process variation are stimulating to create numerous difficulties in the detection of the resistive open defect in memory. For assuring the reliable operation of the circuit, it becomes crucial that memory used in system-on-chip should be fault-tolerant. This paper estimates the efficiency of the proposed Prediscarged feeble cell detection technique used to detect open resistive defect faults in SRAM memory array. The fault detection capabilities are examined for a wide range of defect values at random locations in memory. The implementation of the proposed method gives less time latency and minimum area overhead of 7.74% for 2KB of memory.

Keywords: Fault Detection, Embedded Memory, SRAM Test, Redundant Elements, Resistive Defect.

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INTRODUCTION

The year 2020 will be remembered for Corona or Covid-19 year in future history. In this Covid-19 pandemic situation, everyone is facing lockdown. More than 70% of people in the world are working from home. Almost everyone is using gadgets and laptops with an internet connection. Right from school going child to topmost position people in the industry are using desktop/laptop or gadgets for their work. From online lectures of school or college to international meetings, webinars, training, workshops are taking place on gadgets. Numerous training and informative sessions are getting conducted internationally too with the help of different applications or tools on gadgets. In these, all types of gadgets or device's most important part present is the memory. The standard six transistor Static Random Access Memory (SRAM) cell is shown in Fig. 1. The cell consists of 2 inverters in which M1 and M3 form first inverter and M2 and M4 form second inverter which is connected inversely. The output of the inverters is connected as an input to another inverter so that due to regenerative action of feedback, it can store 1 bit of memory as Q. Its complement output is made available as Q. The lower nmos transistors are called pull-down transistors which pulls the data stored at Q or Q to low. The upper pmos transistors are called pull-up transistors which pulls the data to logic 1. Hence 1-bit data that can be stored as logic 1(0) at $\overline{Q}$ and its complement data 0(1) will be stored as Q. The access transistors (M5 and M6) are used to connect the cell to row and column decoder for read and write operations. Word-line WL is connected to access transistors to activate the cell to access data stored in a cell. Bit-lines BL is used to connect the cell to the sense amplifier and other peripheral circuits for appropriate read and write operations to take place. Such multiple cells form a column structure. Many columns make the SRAM memory array structure. In Very Deep Sub Micron (VDSM) technologies, the size of components like transistors has become so small, but arising with the challenge of process variations, supply voltage, and temperature variations. Applications used in various fields like machine intelligence, cloud computing, internet of things, image processing, video processing, space, biomedical applications require higher reliability. Different types of faults may occur in memory due to manufacturing defects, process variations, electromagnetic radiation, change in temperature, aging of cells due to multiple access, change in bulk voltage, or supply voltage. The type of faults that occurs in cells are stuck at fault, coupling fault, stability faults, open defect fault, etc. Conventional detection of functional failures used to

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detect these faults is not sufficient for memory. In growing Very Deep Sub Micron (VDSM) technologies, the dominant defect emerging is a resistive open defect in memories. The resistive defect may occur at any terminal of all six transistors in the cell as shown in Fig. 2. The resistive defect formed near terminals of pull-up transistors gives hazardous effect to store the data in the cell. These defects make the cell unable to hold the data and make the cell unstable. Similarly, resistive defects present at other terminals emerge to improper read and write operation on cells. So it becomes necessary to detect these faults for the consistent and smooth operation of memory and to make the memory fault-tolerant.

Many methods have come forward for the detection of faults in memory like giving a specific sequence of data for read and write operations on memory to detect the faults. Current and voltage detection methods are also used. But checking the voltage at a pinpoint in memory for fault detection becomes a very tedious job. With the help of minute current disturbance inserting into the memory cell and using sense amplifier to read the data twice for detection of faults is discussed in [1]. The extending period of the word-line signal to detect the faults in memory is shown [2]. Coupling faults between the bit-lines are detected using the read equivalent stress method [3]. Fault detection in the drowsy cache is revealed [4] where memory is operated in drowsy mode. The March test is used for the detection of linked faults [5] by applying various read-write operations in a specific series of packets. Connecting bit-lines to the ground with varied voltage followed by write operation is used to detect the faults in memory [6]. To increase the reliability of memory, a consecutive read cycle on the cells is made forbidden in [7]. A comprehensive summary of different types of March tests is presented in [8]. Dividing logically the cells in columns into different groups and applying a varied number of read cycles to generate voltage for the detection of faults is revealed in [9]. The Built-In Self Repair scheme [10] is used using a bitmap to detect the faults in memory. Quiescent current detection (I_{DDQ}) method is explained using Built-In Current Sensor [11] for the detection of faults in memory. Since the presence of faults changes quiescent current as well as transient current in memory. A study of dynamic fault detection is presented [12] with its causes to occur. Analysis of signal to noise margin for nanometer technologies is discussed in detail [13]. Alike to I_{DDQ} method, the transient current (I_{DDT}) method with some hardware circuitry [14] is also used to detect faults in memory. But in growing advanced VDSM technology, it is very difficult to sense the difference between quiescent or transient current and leakage current. Read disturbance fault detected by the March test is explored in [15]. Changing the supply voltage to source terminals of the devices is used to detect the faults in memory [16]. Fault detection using I_{DDT} current technique is discussed in [17]. By applying the aging effect with the help of a pmos transistor is used to detect the faults in memory [18]. Programmable read and write time instants with word-line underdrive activation method [19] is explored for the detection of faults in memory.

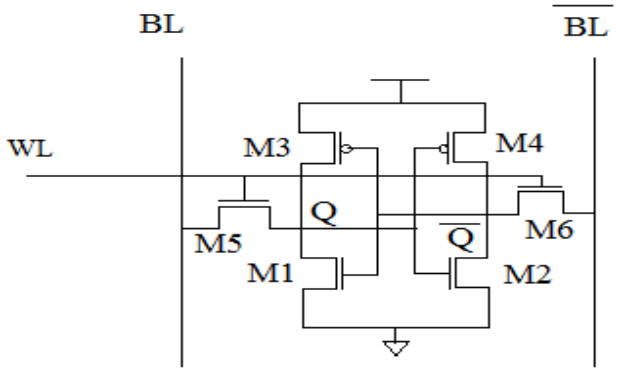

Fig. 1: Standard SRAM Cell Structure

OPEN AND RESISTIVE FAULTS IN SRAM

Sources of Open and Resistive Defect Faults

In the life-time of memory, an infinite number of read and write operations are performed on memory. Power dissipation can be reduced by additional circuit in the cell [22-23]. Due to which aging effect occurs which results in wear and tear of the tracks or connection exist in the memory structure. The effect reforms in resistive defect or open defects in memory. These defects can occur near any terminal of all transistors present in cells as shown in Fig. 2. It may also occur between input and output connections of the inverters as well as near word-line connection. It may plague near the supply connection of the cell or at contacts and vias connection. Open

defect or Resistive defect is caused by weedy contacts or connections. The open defect causes a change in current and voltage in transistors which can be used to detect the faults in memory.

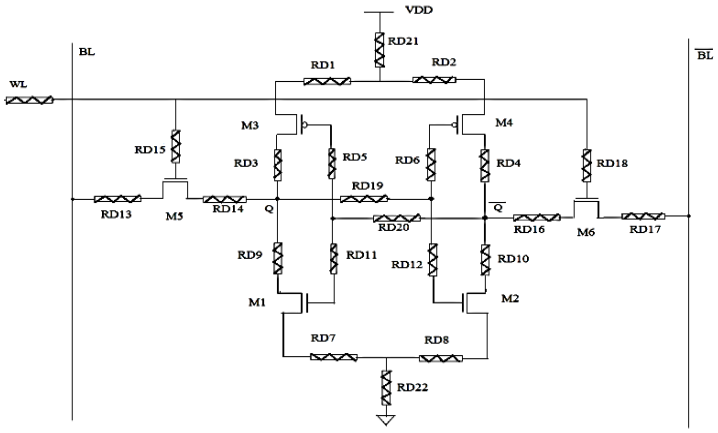

Fig. 2: Resistive Defects in SRAM Cell

The open or resistive defects cause resistance in charging and discharging paths in memory. For example, if the open defect present at the source terminal of the pull-up transistor, the cell wouldn't be able to store the data as logic 1. This results in the stability fault of the memory. The cell couldn't hold the data as logic 1 for a longer period. It gives severe effect on the cell for normal read and write operations of the memory cell. If the resistive fault present near bit-lines, proper pre-discharged voltage couldn't reach the cell, hence causes errors in the read operation. In a write operation, correct data couldn't be written into the cell. Similar effects will occur for the resistive or open defect near supply connections or the word-line connection. For resistive defect present at node terminals Q or Q, appropriate data can't be inputted in the opposite inverter, which causes read and write failure in the memory cell. If the fault present near the source or drain terminals of the pulldown transistor, it gives resistance to the discharging path through access and pull-down transistor. This emerges faulty read operation on memory cell since data couldn't be grounded arise faulty logic 0 read cycle. The faults near pull-up transistors are difficult to detect compared to other location faults in memory. Since pre-charged bit-lines don't experience any change at node terminals, resistive defects at pull-down transistors can be detected by observing the results of the read operation of the memory cell.

Earlier Methods Used for Detection of Faults

Different methods have been used for the detection of open defects or resistive faults in memory. Since open defects have a larger impact on the memory cell, it eases for the detection of faults during read and write operations. As it becomes difficult for charging or discharging operation to takes place. By introducing small current change in the cell followed consecutive read operations by the sense amplifier is used to detect the faults. But this method can detect only the read destructive faults in memory. As well as the assistance of the March test is required for the detection of faults. Sensing the alteration in quiescent current or transient current is used for the detection of faults in memory. But with the advanced technology, reduction in sizing of transistors has increased leakage currents in the memory. As a result, it becomes puzzling to predict that change in currents is arising due to faults or leakage currents. So the current detection method may result in incorrect fault detection in memory. Another method is based on a weak write operation. For the weak write operation, a small voltage difference nearer to ground is established and the cell undergoes write operation. When the fault present in the cell, it results in the flipping of data stored inside the cell. But this technique couldn't detect weak resistive faults in memory. In read equivalent stress method, pre-charged voltage is present on inactive cells too. Hence active and inactive cells undergo repetitive stress given by pre-charge voltage. Then multiple read operations are performed on memory for detection of faults. If the fault is present in the cell, it results in the flipping of data in the cell and faults get detected. Programmable read and write timings are applied with the specific bit-line voltage generated by the read cycle used to detect the fault.

PROPOSED PREDISCHARGED FEEBLE CELL DETECTION METHOD

The design of the SRAM cell is done by taking care of read stability and good write ability with the help of cell ratio and pull-up ratio taken into account. The peripheral circuits are also designed to match the designed cell. For the detection of faults at different locations in the cell, the Pre-discharged feeble cell detection method is proposed. A wide range of resistive defect values is used from 0 ohms to Tera ohm to detect the faults. Open

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defects at each location are also analyzed for the impact on memory cells by changing through infinity. Different locations of resistive defects are considered according to Fig. 2 discussed earlier. A certain sequence of read and write operations is applied for the detection of faults present at various locations in the cell. Bit-line stress on the cell is used for the detection of faults in SRAM in the proposed method. If the cell doesn't contain any fault, it can sustain with stress applied and retain stable data in cells even in consecutive read or write operations.

But when cell consists of the resistive defect, it couldn't resist the bit-line stress applied to it and results in imbalanced situation. The cell becomes incapable to retain the stored logic value and data may get flipped during successive read cycle depending on the value of resistive defect. For resistive defects having less value, faults get detected at lengthier pre-discharged bit-line stress. Whereas for high values of resistive defects, it gets detected with shorter duration bit-line stress. For open defect fault, a high resistive path for current flowing through that terminal makes the detection of fault earlier for SRAM memory. Consecutive read cycles are applied to the cell for the analysis of the type of model of the existed fault in memory. At one time, one type of fault is taken for the analysis as happens in real-time. For resistive defects at different locations in the cell, a range of resistive values is observed to detect the minimum value at which fault is getting detected at that location. Bridging defects at different locations in the cell are also studied. Earlier methods for the detection of faults contain higher area overhead and latency. Some of them even require complex timing circuitry. So it is necessary to develop the fault detection method which gives less time latency and low area overhead for the detection of maximum faults in memory.

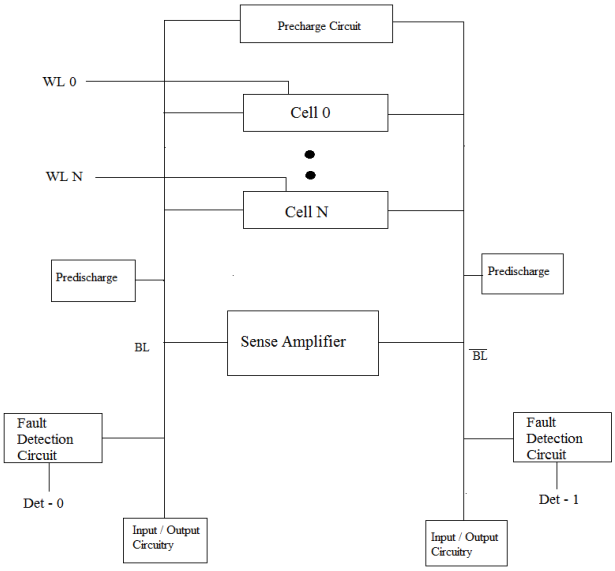

Fig. 3: Block Diagram of Predischarged Feeble Cell Detection

In the proposed method, Predischarged feeble cell detection, when bit-lines attain specific level voltage with the pre-discharge circuit, that voltage is used as stress to detect the faults in memory. Fig. 3 shows the block diagram of the proposed method. The cell under test is activated and undergoes the bit-line stress. The read cycle followed by stress with word-line activation is used to detect the faults in the cell. If the fault is present in the cell, data would get flipped during read or during word-line activation depending on how strong the resistive defect present. A weak resistive defect is also gets detected in word-line activation. The access time obtained for designed memory is 350ps. Open defects are also verified with the proposed technique. The simulation result of the defect located at the source terminal of the PMOS transistor is as shown in Fig. 4. Det-0 and det-1 signals indicate the output of the fault detection circuit. Fig. 5 shows the simulation waveform for the defect located at the source terminal of the NMOS device.

The proposed method verifies the data written into the cell with data read from the cell are the same or any change has occurred in the cell under test. If difference befalls, it is indicated by the circuit. The proposed

method illustrates the improvement in values of minimum detectable resistive defects which is useful to enhance the reliability of memory by early-stage detection of resistive defect faults in memory.

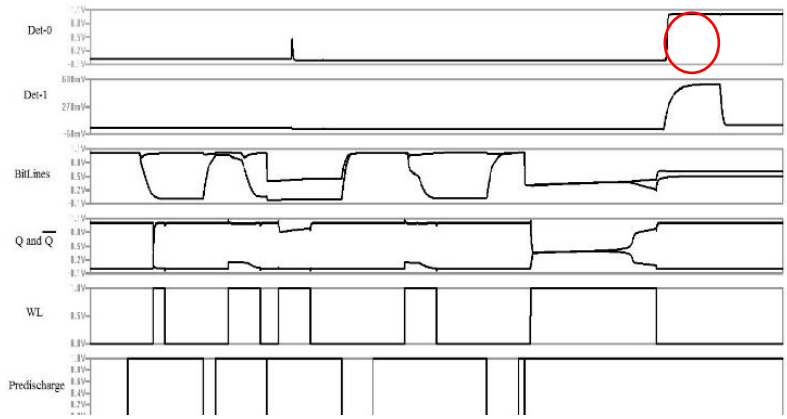

Fig. 4: Simulation Results for Resistive Fault at PMOS Terminal

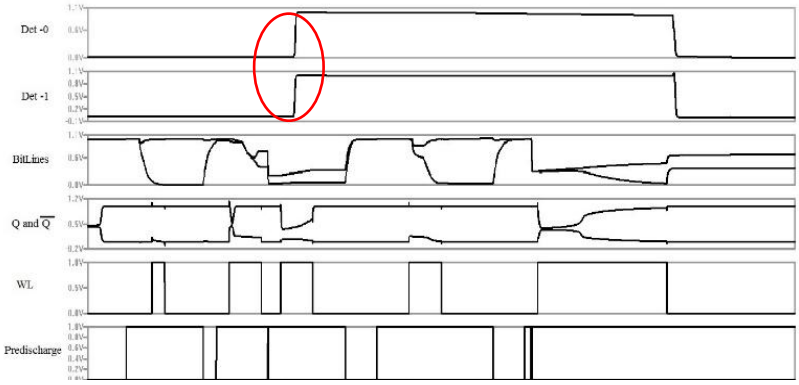

Fig. 5: Simulation Results for Resistive Fault at NMOS Terminal

PERFORMANCE ANALYSIS

To analyse the performance of the proposed pre-discharged feeble cell detection (PDFCD) method, simulations are carried out on the schematic level first. A memory structure 2 KB is designed with 1024 cells in each column. The redundant elements are added in the structure to perform the redundancy analysis. Later, design and simulations are performed using the Cadence virtuoso tool for 45nm technology. Designed memory structure with cells and peripheral circuitry is verified for normal operations with the attached fault detection circuit for optimized access time considering parasitic elements. It is perceived that the access time of memory mainly depends on the parasitic capacitive load present on bit-lines. The simulations performed for normal read and write operations on different cells are as shown in Fig. 6. It shows the access time received is 350ps. Primarily faults emerged at the column level of the circuit for detection.

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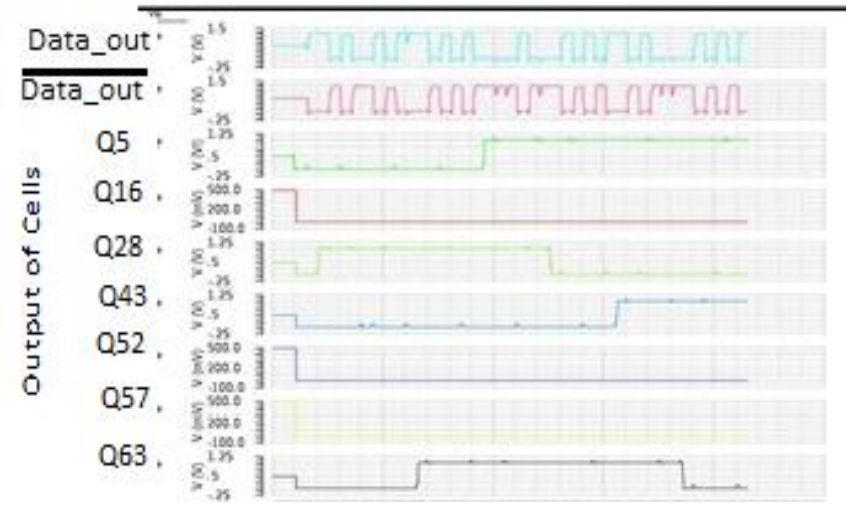

Fig. 6: Simulation Results of SRAM Structure

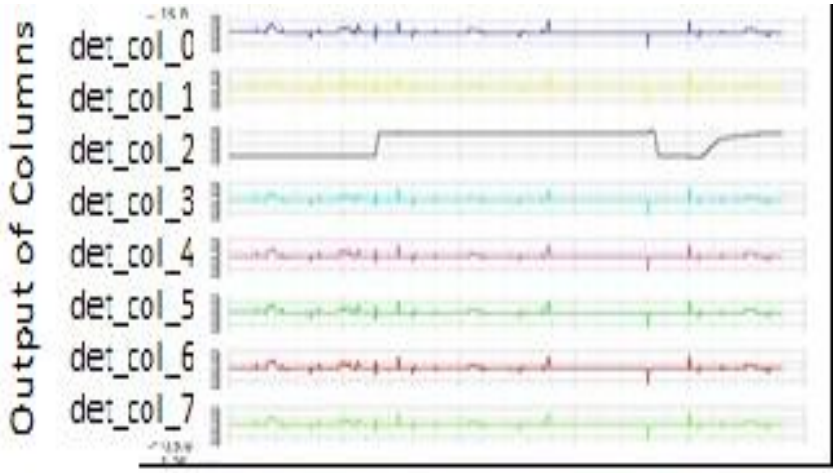

Fig. 7: Simulation Results of Fault Detection in SRAM

Faults have emerged at a random location in column. It is verified that the faults are getting detected at proper locations. Also, output for fault-free cells is checked such that wrong detection shouldn't occur. It is observed that faults are getting detected at all locations in the cell as shown in Fig. 2 with variations applied in values at all locations. Since gate current doesn't hamper much in charging or discharging path, its values are comparably higher. The faults located at supply connections are also verified [20]. After column level, fault detection at the byte level structure is performed. All the steps are again carried out at the byte level. Faults are introduced randomly at different points in different columns. The bridging defects are also verified by using proposed method [21]. The simulation waveform is as shown in Fig. 7. It indicates that fault is present in Column 2 at pull-up transistor. It is taken care that attaching additional fault detection circuit shouldn't hamper normal operations of memory.

RESULTS

The results of simulations for the detection of resistive open defect fault at different locations in the cell are discussed in earlier sections. The design of memory and simulations are executed on 45nm technology Cadence Virtuoso suit. By using the proposed predischarged feeble cell detection method, open resistive defects can be detected for lower values. Resistive open defect value at the source terminal of all 3 types of transistors in the cell is improved compared to current detection technique, hardware-based approach, and complex timing circuitry methods. Table I shows the performance analysis of the proposed method in comparison with other methods. The test time latency achieved by the proposed method is very less compared to other techniques.

Also, the area overhead achieved shows high improvement compared to other methods. Predischarged feeble cell detection illustrates enhanced performance characteristics compared to other methods.

Table 1: Performance Parameters.

Defects	[18]	[14]	Proposed PDFC
Test Time	0.25ms	0.14ms	40.96µs
Area Overhead	-------	5.46%	7.74%

CONCLUSIONS

With the help of Predischarged Feeble Cell Detection, the open resistive defect faults in the memory can be easily detected with improved values. The bridging defects can also be detected by using the proposed method. With the combination of multiple read cycles, the dynamic read destructive fault can be detected as well. The method improves the performance of the circuit with a low area overhead of 7.74% and a lower latency period of 40.96µs for 2KB of memory.

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